FORESEE®

2Gb DDR3L Datasheet

F60C1A0002-M6
Series

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Revision History:

Rev.	Date	Change	Remark
1.0	2019/06	Basic spec and architecture	
1.1	2019/09	Correct Part Number error	
1.2	2019/12	Add 2133Mbps list	
1.3	2019/12	Change the format	
1.4	2019/12	Correct Figure2, Figure3 descriptions	
1.5	2020/09	Remove the space of the PN string	

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Contents

1. INTRODUCTION 5

1.1. General Description 5
1.2. Device Features 5
1.3. Product List 6
1.4. Connection Diagram 7
1.5. Pin Description 7
1.6. System Block Diagram 10

2. COMMAND OPERATION 11

2.1. Command Sets 11
2.2. No Operation Command [NOP] 12
2.3. Device Deselect Command [DESL] 12
2.4. Mode Register Set Command [MR0 to MR3] 12
2.5. Bank Activate Command [ACT] 12
2.6. Read Command [READ, RDS4, RDS8, READA, RDAS4, RDAS8] 12
2.7. Write Command [WRIT, WRS4, WRS8, WRITA, WRAS4, WRAS8] 12
2.8. Precharge Command [PRE, PALL] 12
2.9. Auto precharge Command [READA, WRITA] 13
2.10. Auto-Refresh Command [REF] 13
2.11. Self-Refresh Command [SELF] 13
2.12. ZQ calibration Command [ZQCL, ZQCS] 13
2.13. CKE Truth Table 13

3. Electrical Characteristic 14

3.1. Absolute Maximum Ratings 14
3.2. Operating Temperature Condition 14
3.3. Recommended DC Operating Conditions 14
3.4. 1.35 V DDR3L AC and DC Logic Input Levels for Single-Ended Signals 15
3.5. 1.35 V DDR3L Electrical Characteristics and AC Timing 15
3.6. Address / Command Setup, Hold and Derating 15
3.7. Data Setup, Hold and Slew Rate Derating 15
3.8. Overshoot and Undershoot Specifications 15
3.9. 1.35V DDR3L Output Driver DC Electrical Characteristics 15
3.10. 1.35V DDR3L On-Die Termination (ODT) Levels and I-V Characteristics 15
3.11. 3-11 1.35 V DDR3L Single Ended Output Slew Rate 15
3.12. 3-12 1.35 V Differential Output Slew Rate 15
3.13. 3-13 1.35 V DDR3L AC and DC Logic Input Levels for Differential Signals 15
3.14. 3-14 Differential Input Cross point voltage 15
3.15. 3-15 DQS Output Cross point voltage 16
3.16. DC Characteristics 16
3.17. Self-Refresh Current 17
3.18. Pin Capacitance(TC = 25°C, VDD, VDDQ = 1.35V) 17
3.19. Standard Speed Bins 18
3.20. AC Timing Characteristics 20

4. Functional Description and Timing 25

4.1. Simplified State Diagram 25
4.2. RESET and Initialization Procedure 26
4.3. Programming the Mode Register 27
4.4. DDR3 SDRAM Mode Register 0 [MR0] 29
4.5. DDR3 SDRAM Mode Register 1 [MR1] 30
4.6. DDR3 SDRAM Mode Register 2 [MR2] 31

4.7. DDR3 SDRAM Mode Register 3 [MR3] 32
4.8. Extended Temperature Usage 32
4.9. Refresh Command 33
4.10. Self-Refresh Operation 34
4.11. DLL-off Mode 36
4.12. DLL on/off switching procedure 36
4.13. Input clock frequency change 36
4.14. Write Leveling 36
4.15. Multi Purpose Register 36
4.16. Read Operation 36
4.17. Write Operation 36
4.18. Power-Down Modes 36
4.19. On-Die Termination (ODT) 36
4.20. ZQ Calibration 36

5. Physical Diagram 37

5.1. FBGA 96-ball 7.5mm×13.5mm 37

1. INTRODUCTION

1.1. General Description

The FORESEE DDR3L SDRAM (1.35V) is a low voltage version of the DDR3 (1.5V)SDRAM. Refer to the DDR3 (1.5V) SDRAM datasheet specifications when running in 1.5V compatible mode.

1.2. Device Features

- **Density: 2G bits**
- **Organization**
  - 8 banks x 32M words x 8 bits
  - 8 banks x 16M words x 16 bits
- **Package**
  - 78-ball FBGA
  - 96-ball FBGA
- **Lead-free(RoHS compliant) and Halogen-free**
- **Power supply**
  - VDD, VDDQ =1.35V (1.283 to 1.45V)
  - Backward compatible DDR3 (1.5V) operation
- **Data Rate:**
  1333Mbps/1600Mbps/1866Mbps/2133Mbps
- **1KB page size (x8)**
  - Row address: AX0 to AX14
  - Column address: AY0 to AY9
- **2KB page size (x16)**
  - Row address: AX0 to AX13
  - Column address: AY0 to AY9
- **Eight internal banks for concurrent operation**
- **Burst lengths(BL): 8 and 4 with Burst Chop(BC)**
- **Burst type(BT)**
  - Sequential (8, 4 with BC)
  - Interleave (8, 4 with BC)
- **CAS Latency (CL): 5, 6, 7, 8, 9, 10, 11, 12, 13, 14**
- **CAS Write Latency (CWL): 5, 6, 7, 8, 9, 10**
- **Precharge: auto precharge option for each burst access**
- **Driver strength: RZQ/7, RZQ/6 (RZQ = 240Ω)**
- **Refresh: auto-refresh, self-refresh**
- **Average refresh period**
  - 7.8us at TC ≤ +85℃
  - 3.9us at TC > +85℃
- **Operating temperature range**
  - TC = 0°C to +85°C (Commercial grade)
- **The high-speed data transfer is realized by the 8bits prefetch pipelined architecture**
- **Double data-rate architecture: two data transfers per clock cycle**
- **Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the receiver**
- **DQS is edge-aligned with data for READs; center aligned with data for WRITEs**
- **Differential clock inputs (CK and /CK)**
- **DLL aligns DQ and DQS transitions with CK transitions**
- **Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS**
- **Data mask (DM) for write data**
- **Posted CAS by programmable additive latency for better command and data bus efficiency**
- **On-Die Termination (ODT) for better signal quality**
  - Synchronous ODT
  - Dynamic ODT
  - Asynchronous ODT
- **Multi Purpose Register (MPR) for pre-defined pattern read out**
- **ZQ calibration for DQ drive and ODT Access**
- **Programmable partial array self-refresh (PASR)**
- **RESET pin for Power-up sequence and reset function**
- **SRT(Self Refresh Temperature) range**
  - Normal/Extended/ASR
- **Programmable output driver impedance control**
- **JEDEC compliant DDR3**
- **RH-Free(Row Hammer Free) option is available**

[Table 1]Key Timing Parameters

Data Rate(Mbps)	CL	tRCD	tRP
2133	14	14	14
1866	13	13	13
1600	11	11	11
1333	9	9	9

1.3. Product List

[Table 2] Product List

Part Number	Density	Package Type	Organization	Package Size(mm)	VCC Range	Data Rate(Mbps)
F60C1A0002-M6AR	2Gb	FBGA 96	×16bit	7.5*13.5	1.283V ~ 1.45V	1866
F60C1A0002-M6BR	2Gb	FBGA 96	×16bit	7.5*13.5	1.283V ~ 1.45V	2133

Marketing Part Number Chart

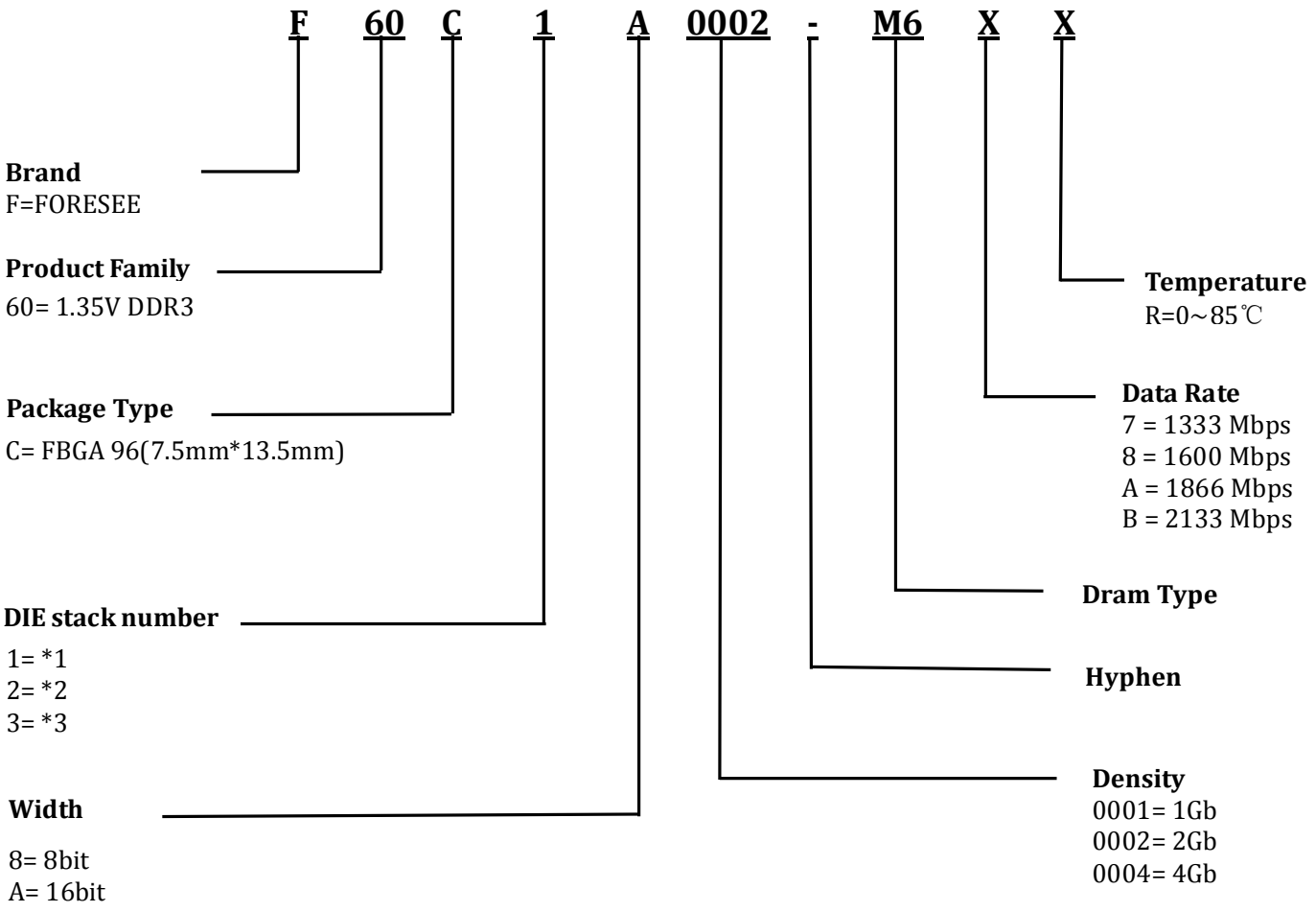


Figure 1 Part Number

1.4. Connection Diagram

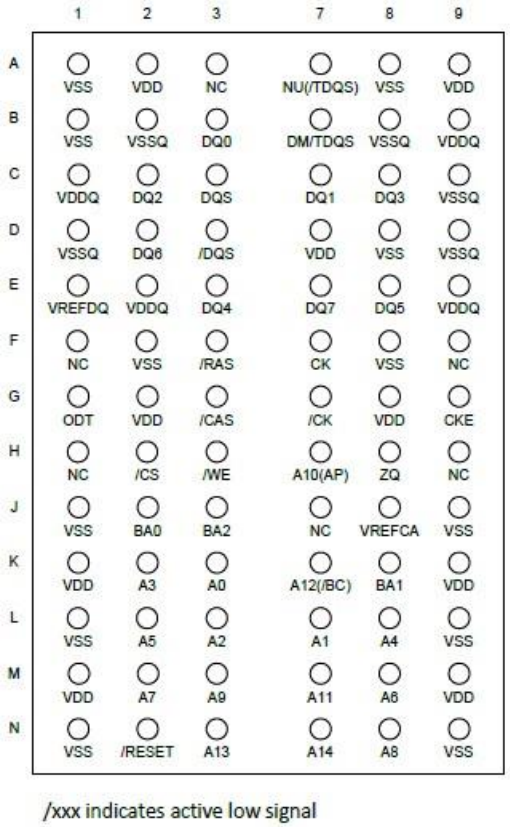


Figure 2 78ball FBGA(x8 organization) top view

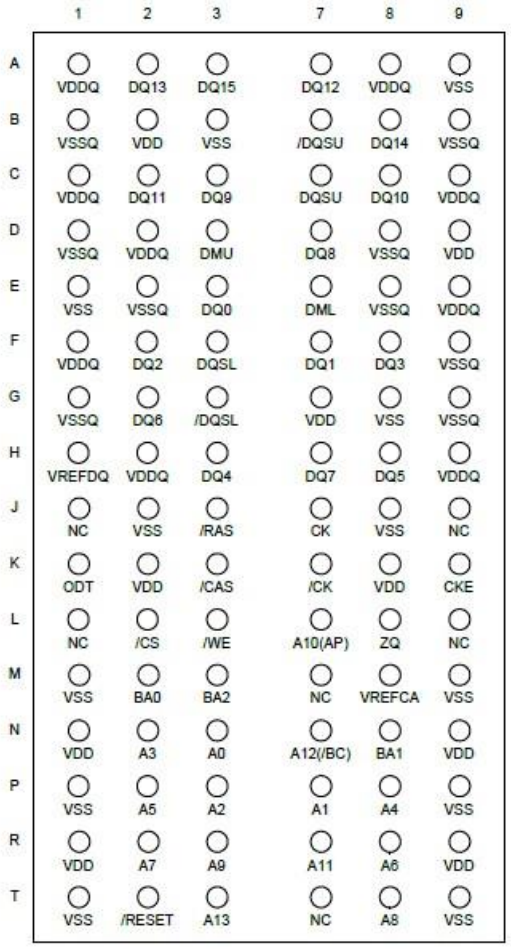


Figure 3 96ball FBGA(x16 organization) top view

1.5. Pin Description

[Table 3] Pin Description

Pin name	Function	Pin name	Function
A0 to A14(×8)*3 A0 to A13(×16)*3	Address inputs A10(AP):Auto precharge A12(/BC):Burst chop	CK,/CK	Differential clock input
		/CS*3	Chip select
		/RAS,/CAS,/WE *3	Command input
BA0 to BA2*3	Bank select	CKE*3	Clock enable
DQ0 to DQ7(×8) DQ0 to DQ15(x16)	Data input/output	ODT*3	ODT control
		VDD	Supply voltage for internal circuit
DQS,/DQS(×8) DQSU,/DQSU,DQSL,/DQSL(×16)	Differential data strobe	VSS	Ground for internal circuit
		VDDQ	Supply voltage for DQ circuit
DM(×8) DMU,DML(×16)	Write data mask	VSSQ	Ground for DQ circuit
		VREFDQ	Reference voltage for DQ
TDQS,/TDQS(×8)	Termination data strobe	VREFCA	Reference voltage for CA
/RESET*3	Active low asynchronous reset	NC*1	No connection
ZQ	Reference pin for ZQ calibration	NU*2	Not Usable

Notes:
[1] Not internally connected with die.
[2] Don't connect. Internally connected.
[3] Input only pins (address, command, CKE, ODT and /RESET) do not supply termination.

CK, /CK (input pins)
CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).

/CS (input pin)
All commands are masked when /CS is registered high. /CS provides for external rank selection on systems with multiple ranks. /CS is considered part of the command code.

/RAS, /CAS, /WE (input pins)
/RAS, /CAS and /WE (along with /CS) define the command being entered.

A0 to A14 (input pins)
Provided the row address for active commands and the column address for read/write commands to select one location out of the memory array in the respective bank. (A10(AP) and A12(/BC) have additional functions, see below) The address inputs also provide the op-code during mode register set commands.

[Table 4] Address Pins

Configuration	Page Size	Address (A0 to A14)		Note
		Row address	Column address	
×8	1KB	AX0 to AX14	AY0 to AY9	
×16	2KB	AX0 to AX13	AY0 to AY9	

A10(AP) (input pin)
A10 is sampled during read/write commands to determine whether auto precharge should be performed to the accessed bank after the read/write operation. (high: auto precharge; low: no auto precharge) A10 is sampled during a precharge command to determine whether the precharge applies to one bank (A10 = low) or all banks (A10 = high). If only one bank is to be precharged, the bank is selected by bank addresses (BA).

A12(/BC) (input pin)
A12 is sampled during read and write commands to determine if burst chop (on-the-fly) will be performed. (A12 = high: no burst chop, A12 = low: burst chopped.) See command truth table for details.

BA0 to BA2 (input pins)
BA0, BA1 and BA2 define to which bank an active, read, write or precharge command is being applied. BA0 and BA1 also determine which mode register (MR0 to MR3) is to be accessed during a MRS cycle.

[Table 5] Bank select

Bank	BA2	BA1	BA0
Bank0	L	L	L
Bank1	L	L	H
Bank2	L	H	L
Bank3	L	H	H
Bank4	H	L	L
Bank5	H	L	H
Bank6	H	H	L
Bank7	H	H	H

Remark: H: VIH, L: VIL

CKE (input pin)
CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides precharge power-down and self-refresh operation (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self-refresh exit. After VREF has become stable during the power-on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, VREF must be maintained to this input. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, /CK, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self-refresh.

DM, DMU, DML (input pins)
DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a write access. DM is sampled on both edges of DQS.

DQ0 to DQ15 (input/output pins)
Bi-directional data bus.

DQS, /DQS, DQSU, /DQSU, DQSL, /DQSL (input/output pins)
Output with read data, input with write data. Edge-aligned with read data, center-aligned with write data. The data strobe DQS is paired with differential signal /DQS to provide differential pair signaling to the system during READs and WRITEs.

/RESET (input pin)
/RESET is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD (1.20V for DC high and 0.30V for DC low). It is negative active signal (active low) and is referred to GND. There is no termination required on this signal. It will be heavily loaded across multiple chips.
/RESET is destructive to data contents.

ODT (input pin)
ODT (registered high) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is applied to each DQ, DQSU, /DQSU, DQSL, /DQSL, DMU, and DML signal. The ODT pin will be ignored if the mode register (MR1) is programmed to disable ODT.

ZQ (supply)
Reference pin for ZQ calibration.

VDD, VSS, VDDQ, VSSQ (power supply pins)
VDD and VSS are power supply pins for internal circuits. VDDQ and VSSQ are power supply pins for the output buffers.

VREFCA, VREFDQ (power supply pins)
Reference voltage.

1.6. System Block Diagram

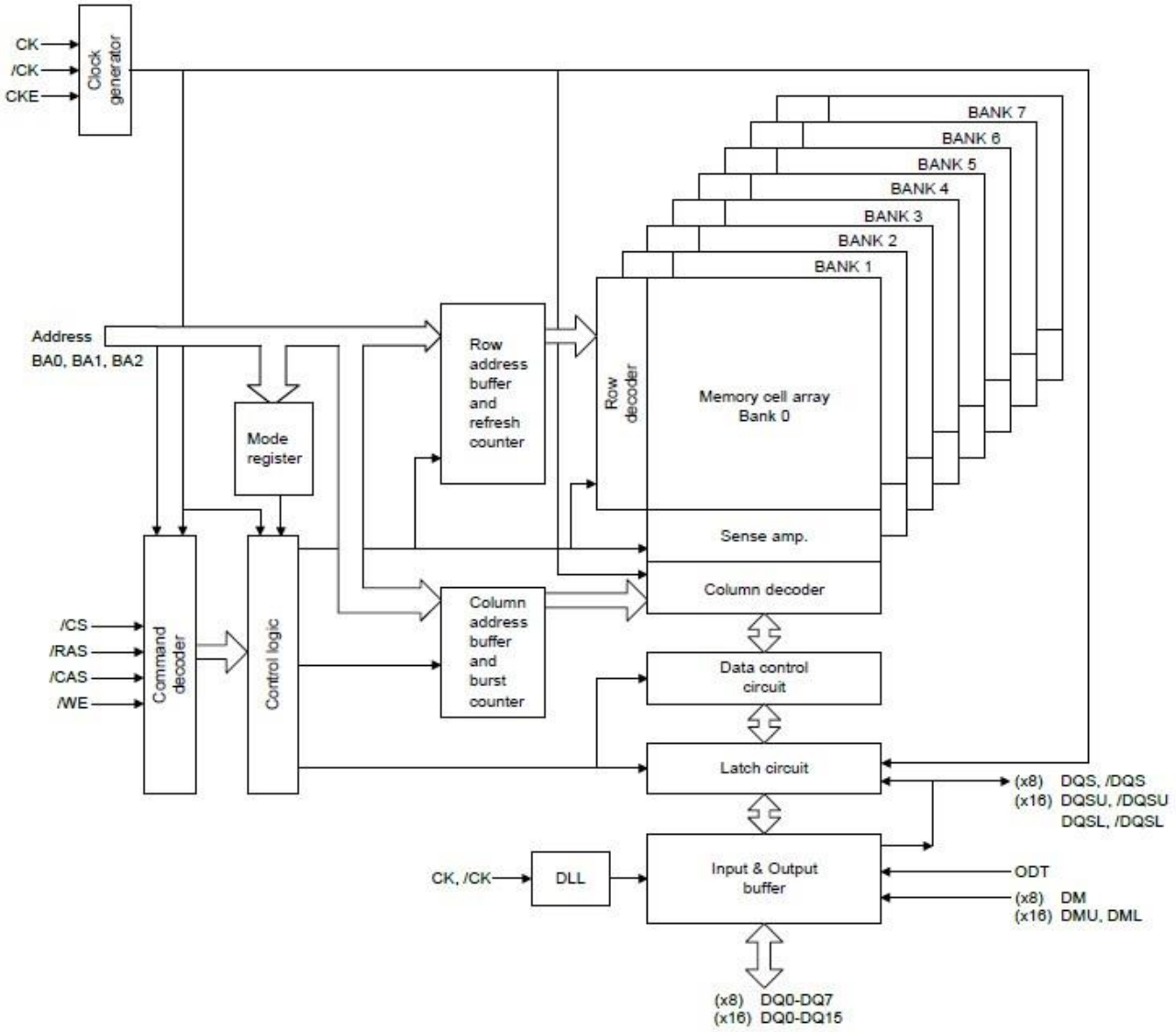


Figure 4 DDR3L Functional Block Diagram

2. COMMAND OPERATION

2.1. Command Sets

The DDR3 SDRAM recognizes the following commands specified by the /CS, /RAS, /CAS, /WE and address pins.

[Table 6] Command Truth Table

Function	Symbol	CKE		/CS	/RAS	/CAS	/WE	BA0-2	A12(/BS)	A10(AP)	A0-A14	Note
		Previous	Current									
Mode register set	MRS	H	H	L	L	L	L	BA	op-code			
Auto refresh	REF	H	H	L	L	L	H	V	V	V	V	
Self refresh entry	SELF	H	L	L	L	L	H	V	V	V	V	6,8,11
Self refresh exit	SELEX	L	H	H	X	X	X	X	X	X	X	6,8,7
		L	H	L	H	H	H	V	V	V	V	11
Single bank precharge	PRE	H	H	L	L	H	L	BA	V	L	V	
Precharge all banks	PALL	H	H	L	L	H	L	V	V	H	V	
Bank activate	ACT	H	H	L	L	H	H	BA	RA			12
Write(Fixed BL) Write(BC4,on the fly) Write(BL8,on the fly)	WRIT	H	H	L	H	L	L	BA	V	L	CA	
	WRS4	H	H	L	H	L	L	BA	L	L	CA	
	WRS8	H	H	L	H	L	L	BA	H	L	CA	
Write with auto precharge (Fixed BL)	WRITA	H	H	L	H	L	L	BA	V	H	CA	
Write with auto precharge (BC4,on the fly)	WRAS4	H	H	L	H	L	L	BA	L	H	CA	
Write with auto precharge (BL8,on the fly)	WRAS8	H	H	L	H	L	L	BA	H	H	CA	
Read(Fixed BL)	READ	H	H	L	H	L	H	BA	V	L	CA	
Read(BC4,on the fly)	RDS4	H	H	L	H	L	H	BA	L	L	CA	
Read(BL8,on the fly)	RDS8	H	H	L	H	L	H	BA	H	L	CA	
Read with auto precharge (Fixed BL)	READA	H	H	L	H	L	H	BA	V	H	CA	
Read with auto precharge (BC4,on the fly)	RDAS4	H	H	L	H	L	H	BA	L	H	CA	
Read with auto precharge (BL8,on the fly)	RDAS8	H	H	L	H	L	H	BA	H	H	CA	
No operation	NOP	H	H	L	H	H	H	V	V	V	V	9
Device deselect	DESL	H	H	H	X	X	X	X	X	X	X	10
Power down mode entry	PDEN	H	L	H	X	X	X	X	X	X	X	5,11
		H	L	L	H	H	H	V	V	V	V	
Power down mode exit	PDEX	L	H	H	X	X	X	X	X	X	X	5,11
		L	H	L	H	H	H	V	V	V	V	
ZQ calibration long	ZQCL	H	H	L	H	H	L	X	X	H	X	
ZQ calibration short	ZQCS	H	H	L	H	H	L	X	X	L	X	

Remark:
[1] H = VIH; L = VIL; V =VIH or VIL(defined logical level).
[2] X = Don't care (defined or undefined, including floating around VREF) logical level. [3] BA = Bank Address. RA = Row Address. CA = Column Address. /BC = Bust Chop.

Notes:
[1] All DDR3 commands are defined by states of /CS, /RAS, /CAS, /WE and CKE at the rising edge of the clock. The most significant bit (MSB) of BA, RA, and CA are device density and configuration dependent.
[2] /RESET is an active low asynchronous signal that must be driven high during normal operation.
[3] Bank Addresses (BA) determines which bank is to be operated upon. For MRS, BA selects a mode register.
[4] Burst READs or WRITEs cannot be terminated or interrupted and fixed/on the fly BL will be defined by MRS.
[5] The power-down mode does not perform any refresh operations.
[6] The state of ODT does not affect the states described in this table. The ODT function is not available during self-refresh.
[7] Self-refresh exit is asynchronous.
[8] VREF (both VREFDQ and VREFCA) must be maintained during self-refresh operation. VREFDQ supply may be turned off and VREFDQ may take any value between VSS and VDD during self-refresh operation, provided that VREFDQ is valid and stable prior to CKE going back high and that first write operation or first write leveling activity may not occur earlier than 512 nCK after exit from self-refresh.
[9] The No Operation command (NOP) should be used in cases when the DDR3 SDRAM is in an idle or a wait state. The purpose of the NOP command is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A NOP command will not terminate a previous operation that is still executing, such as a burst read or write cycle.
[10] The DESL command performs the same function as a NOP command.
[11] Refer to the CKE Truth Table for more detail with CKE transition.
[12]. No more than 4 banks may be activated in a rolling tFAW window. Converting to clocks is done by dividing tFAW (ns) by tCK (ns) and rounding up to next

integer value. As an example of the rolling window, if (tFAW/tCK) rounds up to 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued in clock N+1 through N+9.

2.2. No Operation Command [NOP]

The No Operation command (NOP) should be used in cases when the DDR3 SDRAM is in an idle or a wait state. The purpose of the NOP command is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A NOP command will not terminate a previous operation that is still executing, such as a burst read or write cycle.
The no operation (NOP) command is used to instruct the selected DDR3 SDRAM to perform a NOP (/CS low, /RAS, /CAS, /WE high). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

2.3. Device Deselect Command [DESL]

The deselect function (/CS high) prevents new commands from being executed by the DDR3 SDRAM. The DDR3 SDRAM is effectively deselected. Operations already in progress are not affected.

2.4. Mode Register Set Command [MR0 to MR3]

The mode registers are loaded via row address inputs. See mode register descriptions in the Programming the mode register section. The mode register set command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until tMRD is met.

2.5. Bank Activate Command [ACT]

This command is used to open (or activate) a row in a particular bank for a subsequent access. The values on the BA inputs select the bank, and the address provided on row address inputs selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank. A precharge command must be issued before opening a different row in the same bank.

Note: No more than 4 banks may be activated in a rolling tFAW window. Converting to clocks is done by dividing tFAW (ns) by tCK (ns) and rounding up to next integer value. As an example of the rolling window, if (tFAW/tCK) rounds up to 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued in clock N+1 through N+9.

2.6. Read Command [READ, RDS4, RDS8, READA, RDAS4, RDAS8]

The read command is used to initiate a burst read access to an active row. The values on the BA inputs select the bank, and the address provided on column address inputs selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

2.7. Write Command [WRIT, WRS4, WRS8, WRITA, WRAS4, WRAS8]

The write command is used to initiate a burst write access to an active row. The values on the BA inputs select the bank, and the address provided on column address inputs selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered low, the corresponding data will be written to memory; if the DM signal is registered high, the corresponding data inputs will be ignored, and a write will not be executed to that byte/column location.

2.8. Precharge Command [PRE, PALL]

The precharge command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA select the bank. Otherwise BA are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any read or write commands being issued to that bank. A precharge command will be treated as a NOP if there is no open row in that bank (idle state), or if the previously open row is already in the process of precharging.

2.9. Auto precharge Command [READA, WRITA]

Before a new row in an active bank can be opened, the active bank must be precharged using either the precharge command or the auto precharge function. When a read or a write command is given to the DDR3 SDRAM, the /CAS timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is low when the read or write command is issued, then normal read or write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is high when the read or write command is issued, then the auto precharge function is engaged. During auto precharge, a read command will execute as normal with the exception that the active bank will begin to precharge on the rising edge which is (AL* + tRTP) cycles later from the read with auto precharge command.
Auto precharge can also be implemented during write commands. The precharge operation engaged by the Auto precharge command will not begin until the last data of the burst write sequence is properly stored in the memory array.
This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon /CAS latency) thus improving system performance for random data access. The tRAS lockout circuit internally delays the Precharge operation until the array restore operation has been completed so that the auto precharge command may be issued with any read or write command.
Note: AL (Additive Latency), refer to Posted /CAS description in the Register Definition section.

2.10. Auto-Refresh Command [REF]

Auto-refresh is used during normal operation of the DDR3 SDRAM and is analogous to /CAS-before-/RAS (CBR) refresh in FPM/EDO DRAM. This command is nonpersistent, so it must be issued each time a refresh is required. The addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during an auto-refresh command.
A maximum of eight auto-refresh commands can be posted to any given DDR3, meaning that the maximum absolute interval between any auto-refresh command and the next auto-refresh command is 9 x tREFI. This maximum absolute interval is to allow DDR3 output drivers and internal terminators to automatically recalibrate compensating for voltage and temperature changes.

2.11. Self-Refresh Command [SELF]

The self-refresh command can be used to retain data in the DDR3, even if the rest of the system is powered down. When in the self-refresh mode, the DDR3 retains data without external clocking. The self-refresh command is initiated like an auto-refresh command except CKE is disabled (low).
The DLL is automatically disabled upon entering self-refresh and is automatically enabled and reset upon exiting self-refresh. The active termination is also disabled upon entering self-refresh and enabled upon exiting self-refresh. (512 clock cycles must then occur before a read command can be issued). Input signals except CKE are "Don't Care" during self-refresh. The procedure for exiting self-refresh requires a sequence of commands.
First, CK and /CK must be stable prior to CKE going back high. Once CKE is high, the DDR3 must have NOP commands issuedfor tXSDLL because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh, DLL requirements and out-put calibration is to apply NOPs for 512 clock cycles before applying any other command to allow the DLL to lock and the output drivers to recalibrate.

2.12. ZQ calibration Command [ZQCL, ZQCS]

ZQ calibration command (short or long) is used to calibrate DRAM RON and ODT values over PVT. ZQ Calibration Long (ZQCL) command is used to perform the initial calibration during power-up initialization sequence.
ZQ Calibration Short (ZQCS) command is used to perform periodic calibrations to account for VT variations. All banks must be precharged and tRP met before ZQCL or ZQCS commands are issued by the controller.
ZQ calibration commands can also be issued in parallel to DLL lock time when coming out of self-refresh.

2.13. CKE Truth Table

[Refer to section 4.2 in JEDEC Standard No. JESD79-3F]

3. Electrical Characteristic

All voltages are referenced to each VSS (GND).
Execute power-up and Initialization sequence before proper device operation can be achieved.

3.1. Absolute Maximum Ratings

[Table 7] Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Power supply voltage	VDD	-0.4 to +1.975	V	1,3
Power supply voltage for output	VDDQ	-0.4 to +1.975	V	1,3
Input voltage	VIN	-0.4 to+1.975	V	1
Output voltage	VOUT	-0.4 to+1.975	V	1
Reference voltage	VREFCA	-0.4 to 0.6×VDD	V	3
Reference voltage for DQ	VREFDQ	-0.4 to 0.6xVDDQ	V	3
Storage temperature	Tstg	-55 to+150	℃	1,2
Power dissipation	PD	1.0	W	1
Short circuit output current	IOUT	50	mA	1

Notes:
[1] Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
[2] Storage temperature is the case surface temperature on the center/top side of the DRAM.
[3] VDD and VDDQ must be within 300mV of each other at all times; and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

Caution:
Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

3.2. Operating Temperature Condition

[Table 8] Operating Temperature Condition

Product grades	Parameter	Symbol	Rating	Unit	Note
Commercial	Operating case temperature	TC	0 to +85	℃	1,2,3

Notes:
[1] Operating temperature is the case surface temperature on the center/top side of the DRAM.
[2] The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0°C to +85°C under all operating conditions.
[3] Some applications require operation of the DRAM in the Extended Temperature Range between +85°C and +95°C (and +105°C for automotive grade only) case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply.
[4] Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9µs.
[5] If Self-refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 bit [A6, A7] = [0, 1]) or enable the optional Auto Self-Refresh mode (MR2 bit [A6, A7] = [1, 0]).

3.3. Recommended DC Operating Conditions

[Table 9] Recommended DC operating Conditions for DDR3L (1.35V)

Parameter	Symbol	min.	typ.	max.	Unit	Note
Supply voltage	VDD	1.283	1.35	1.45	V	1,2
Supply voltage for DQ	VDDQ	1.283	1.35	1.45	V	1,2

Notes:
[1] Maximum DC value may not be greater than 1.425V. The DC value is the linear average of VDD/VDDQ(t) over a very long period of time (e.g. 1sec.).
[2] If maximum limit is exceeded, input levels shall be governed by DDR3 specifications.
[3] Under these supply voltages, the device operates to this DDR3L specification.
[4] Once initialized for DDRD3L operation, DDR3 operation may only be used if the device is in reset while.
[5] VDD and VDDQ are changed for DDR3 operation shown as following timing waveform.

[Table 10] Recommended DC operating Conditions for DDR3L (1.5V)

Parameter	Symbol	min.	typ.	max.	Unit	Note
Supply voltage	VDD	1.425	1.5	1.575	V	1,2
Supply voltage for DQ	VDDQ	1.425	1.5	1.575	V	1,2

Notes:
[1] If minimum limit is exceeded, input levels shall be governed by DDR3L specifications.
[2] Under 1.5V operation, the DDR3L device operates to the DDR3 specification under the same speed timings as defined for this device.
[3] Once initialized for DDR3 operation, DDR3L operation may only be used if the device in reset while VDD and VDDQ are changed for DDR3L operation shown as next page.

3.4. 1.35 V DDR3L AC and DC Logic Input Levels for Single-Ended Signals

[Refer to section 3 in JEDEC Standard No. JESD79- 3- 1A.01]

3.5. 1.35 V DDR3L Electrical Characteristics and AC Timing

[Refer to section 4 in JEDEC Standard No. JESD79- 3- 1A.01]

3.6. Address / Command Setup, Hold and Derating

[Refer to section 4.1 in JEDEC Standard No. JESD79- 3- 1A.01]

3.7. Data Setup, Hold and Slew Rate Derating

[Refer to section 4.2 in JEDEC Standard No. JESD79- 3- 1A.01]

3.8. Overshoot and Undershoot Specifications

[Refer to section 9.6 in JEDEC Standard No. JESD79-3F]

3.9. 1.35V DDR3L Output Driver DC Electrical Characteristics

[Refer to section 6 in JEDEC Standard No. JESD79- 3- 1A.01]

3.10. 1.35V DDR3L On-Die Termination (ODT) Levels and I-V Characteristics

[Refer to section 7 in JEDEC Standard No. JESD79- 3- 1A.01]

3.11. 3-11 1.35 V DDR3L Single Ended Output Slew Rate

[Refer to section 8 in JEDEC Standard No. JESD79- 3- 1A.01]

3.12. 3-12 1.35 V Differential Output Slew Rate

[Refer to section 9 in JEDEC Standard No. JESD79- 3- 1A.01]

3.13. 3-13 1.35 V DDR3L AC and DC Logic Input Levels for Differential Signals

[Refer to section 10 in JEDEC Standard No. JESD79- 3- 1A.01]

3.14. 3-14 Differential Input Cross point voltage

[Refer to section 11 in JEDEC Standard No. JESD79- 3- 1A.01]

3.15. 3-15 DQS Output Cross point voltage

[Refer to section 12 in JEDEC Standard No. JESD79- 3- 1A.01]

3.16. DC Characteristics

[Table 11] DC Characteristics

Parameter	Symbol	Data rate (Mbps)	×8(1.35V) max.	×8(1.5V) max.	×16(1.35V) max.	×16(1.5V) max.	Unit	Notes
Operating current (ACT-PRE)	IDD0	2133	TBD	TBD	59	59	mA	
		1866	TBD	TBD	57	57		
		1600	TBD	TBD	55	55		
		1333	TBD	TBD	53	53		
Operating current (ACT-READ-PRE)	IDD1	2133	TBD	TBD	85	85	mA	
		1866	TBD	TBD	82	82		
		1600	TBD	TBD	79	79		
		1333	TBD	TBD	77	77		
Precharge power-down Standby current	IDD2P1	2133	TBD	TBD	16	16	mA	Fast PD Exit
		1866	TBD	TBD	14	14		
		1600	TBD	TBD	12	12		
		1333	TBD	TBD	10	10		
	IDD2P0	2133	TBD	TBD	7	7	mA	Slow PD Exit
		1866	TBD	TBD	7	7		
		1600	TBD	TBD	7	7		
		1333	TBD	TBD	7	7		
Precharge standby current	IDD2N	2133	TBD	TBD	26	26	mA	
		1866	TBD	TBD	24	24		
		1600	TBD	TBD	22	22		
		1333	TBD	TBD	20	20		
Precharge standby current ODT current	IDD2NT	2133	TBD	TBD	33	33	mA	
		1866	TBD	TBD	31	31		
		1600	TBD	TBD	29	29		
		1333	TBD	TBD	27	27		
Precharge quiet standby Current	IDD2Q	2133	TBD	TBD	26	26	mA	
		1866	TBD	TBD	24	24		
		1600	TBD	TBD	22	22		
		1333	TBD	TBD	20	20		
Active power-down current(Always fast exit)	IDD3P	2133	TBD	TBD	28	28	mA	
		1866	TBD	TBD	26	26		
		1600	TBD	TBD	24	24		
		1333	TBD	TBD	22	22		
Active standby current	IDD3N	2133	TBD	TBD	40	40	mA	
		1866	TBD	TBD	38	38		
		1600	TBD	TBD	36	36		
		1333	TBD	TBD	34	34		
Operating current(Burst read operating)	IDD4R	2133	TBD	TBD	173	173	mA	
		1866	TBD	TBD	163	163		
		1600	TBD	TBD	153	153		
		1333	TBD	TBD	143	143		
Operating current(Burst write operating)	IDD4W	2133	TBD	TBD	173	173	mA	
		1866	TBD	TBD	163	163		
		1600	TBD	TBD	153	153		
		1333	TBD	TBD	143	143		
Burst refresh current	IDD5B	2133	TBD	TBD	247	247	mA	
		1866	TBD	TBD	240	240		
		1600	TBD	TBD	233	233		
		1333	TBD	TBD	226	226		
All bank interleave read current	IDD7	2133	TBD	TBD	208	208	mA	
		1866	TBD	TBD	198	198		
		1600	TBD	TBD	188	188		
		1333	TBD	TBD	178	178		
RESET low current	IDD8	-	TBD	TBD	ldd2P+2	ldd2P+2	mA	

Notes :
[1]VIL can undershoot to -0.4V and VIH can overshoot to VCC +0.4V for durations of 20ns or less.
[2]Typical value is measured at VCC=3.3V, TA=25℃. Not 100% tested.

3.17. Self-Refresh Current

[Refer to section 10 in JEDEC Standard No. JESD79-3F for detailed test condition]
[Table 12] Self-Refresh Current

Parameter	Symbol	×8(1.35V)	×8(1.5V)	×16(1.35V)	×16(1.5V)	Unit	Notes
		max.	max.	max.	max.		
Self-refresh current Normal temperature range	IDD6	TBD	TBD	10	10	mA	
Self-refresh current Extended temperature range	IDD6E	TBD	TBD	14	14	mA	

Notes:
[1] For Automotive grade products, when TC > 95℃, all IDD excepting IDD6 must be increased by 20%.
[2] For RH-Free options, the IDD5B must be increased 30%, IDD6 and IDD6E must be increased by 50%.

3.18. Pin Capacitance(TC = 25°C, VDD, VDDQ = 1.35V)

[Table 13] Pin Capacitance

Parameter	Symbol	DDR3L -1333		DDR3L -1600		DDR3L -1866		DDR3L -2133		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Input/output capacitance	CIO	1.4	2.3	1.4	2.2	1.4	2.1	1.4	2.1	pF	1,2
Input capacitance,CK and /CK	CCK	0.8	1.4	0.8	1.4	0.8	1.4	0.8	1.4	pF	2
Input capacitance delta, CK and/CK	CDCK	0	0.15	0	0.15	0	0.15	0	0.15	pF	2,3
Input/output capacitance delta,DQS and/DQS	CDDQS	0	0.15	0	0.15	0	0.15	0	0.15	pF	2,4
Input capacitance, (control,address, command,input-only pins)	CI	0.75	1.3	0.75	1.2	0.75	1.2	0.75	1.2	pF	2,5
Input capacitance delta, (all control input-only pins)	CDI_CTRL	-0.4	0.2	-0.4	0.2	-0.4	0.2	-0.4	0.2	pF	2,6,7
|Input capacitance delta, (all address/command input-only pins)	CDI_ADD_CMD	-0.4	0.4	-0.4	0.4	-0.4	0.4	-0.4	0.4	pF	2,8,9
Input/output capacitance delta,DQ,DM,DQS,/DQS, TDQS,/TDQS	CDIO	-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	2,10
Input/output capacitance of ZQ pin	CZQ	-	3	-	3	-	3	-	3	pF	2,11

Notes:
[1]. Although the DM, TDQS and /TDQS pins have different functions, the loading matches DQ and DQS.
[2] VDD, VDDQ, VSS, VSSQ applied and all other pins floating (excepting the pin under test, CKE, /RESET and ODT as necessary). VDD = VDDQ =1.35V, VBIAS=VDD/2 and on die termination off.
[3] Absolute value of CCK(CK) - CCK(/CK).
[4] Absolute value of CIO(DQS) - CIO(/DQS).
[5] CI applies to ODT, /CS, CKE, A0-A15, BA0-BA2, /RAS, /CAS and /WE.
[6] CDI_CTRL applies to ODT, /CS and CKE.
[7] CDI_CTRL = CI(CTRL) - 0.5 x (CI(CK)+CI(/CK)).
[8] CDI_ADD_CMD applies to A0-A15, BA0-BA2, /RAS, /CAS and /WE.
[9] CDI_ADD_CMD = CI(ADD_CMD) - 0.5 x (CI(CK) + CI(/CK)).
[10] CDIO = CIO(DQ, DM) - 0.5 x (CIO(DQS) + CIO(/DQS)).
[11] Maximum external load capacitance on ZQ pin: 5pF.

3.19. Standard Speed Bins

Refer to section 12.3 in JEDEC Standard No. JESD79-3F.

[Table 14] Standard Speed Bins

Speed Bin			DDR3L-1333		DDR3L-1600		DDR3L-1866		Unit
CL-tRCD-tRP			9-9-9		11-11-11		13-13-13		
Parameter		Symobl	Min.	Max.	Min.	Max.	Min.	Max.	
Internal read command to first data		tAA	13.5 (13.125)	20.0	13.75 (13.125)	20.0	13.91 (13.125)	20.0	ns
ACT to internal read or write delay time		tRCD	13.5 (13.125)	-	13.75 (13.125)	-	13.91 (13.125)	-	ns
PRE command period		tRP	13.5 (13.125)	-	13.75 (13.125)	-	13.91 (13.125)	-	ns
ACT to ACT or REF command period		tRC	49.5 (49.125)	-	48.75 (48.125)	-	47.91 (47.125)	-	ns
ACT to PRE command period		tRAS	36	9xtREFI	35	9xtREFI		9xtREFI	ns
CL=5	CWL=5	tCK (avg)	3.0	3.3	3.0	3.3	3.0	3.3	ns
	CWL=6,7,8,9	tCK (avg)	Reserved		Reserved		Reserved		ns
CL=6	CWL=5	tCK (avg)	2.5	3.3	2.5	3.3	2.5	3.3	ns
	CWL=6	tCK (avg)	Reserved		Reserved		Reserved		ns
	CWL=7,8,9	tCK (avg)	Reserved		Reserved		Reserved		ns
CL=7	CWL=5	tCK (avg)	Reserved		Reserved		Reserved		ns
	CWL=6	tCK (avg)	1.875	<2.5	1.875	<2.5	1.875	<2.5	ns
	CWL=7,8,9	tCK (avg)	Reserved		Reserved		Reserved		ns
CL=8	CWL=5	tCK (avg)	Reserved		Reserved		Reserved		ns
	CWL=6	tCK (avg)	1.875	<2.5	1.875	<2.5	1.875	<2.5	ns
	CWL=7,8,9	tCK (avg)	Reserved		Reserved		Reserved		ns
CL=9	CWL=5,6	tCK (avg)	Reserved		Reserved		Reserved		ns
	CWL=7	tCK (avg)	1.5	<1.875	1.5	<1.875	1.5	<1.875	ns
	CWL=8,9	tCK (avg)	Reserved		Reserved		Reserved		ns
CL=10	CWL=5,6	tCK (avg)	Reserved		Reserved		Reserved		ns
	CWL=7	tCK (avg)	1.5	<1.875	1.5	<1.875	1.5	<1.875	ns
	CWL=8,9	tCK (avg)	Reserved		Reserved		Reserved		ns
CL=11	CWL=5,6,7	tCK (avg)	Reserved		Reserved		Reserved		ns
	CWL=8	tCK (avg)	Reserved		1.25	<1.5	1.25	<1.5	ns
	CWL=9	tCK (avg)	Reserved		Reserved		Reserved		ns
CL=12	CWL=5,6,7,8,9	tCK (avg)	Reserved		Reserved		Reserved		ns
CL=13	CWL=5,6,7,8	tCK (avg)	Reserved		Reserved		Reserved		ns
	CWL=9	tCK (avg)	Reserved		Reserved		1.07	<1.25	ns
Supported CL settings			5,6,7,8,9,10		5,6,7,8,9,10,11		5,6,7,8,9,10,11,13		nCK
Supported CWL settings			5,6,7		5,6,7,8		5,6,7,8,9		nCK

[Table 14] Standard Speed Bins(continue)

Speed Bin			DDR3L-1866		Unit
CL-tRCD-tRP			13-13-13		
Parameter		Symobl	Min.	Max.	
Internal read command to first data		tAA	13.09	20.0	ns
ACT to internal read or write delay time		tRCD	13.09	-	ns
PRE command period		tRP	13.09	-	ns
ACT to ACT or REF command period		tRC	46.09	-	ns
ACT to PRE command period		tRAS	33	9xtREFI	ns
CL=5	CWL=5	tCK (avg)	Reserved		ns
	CWL=6,7,8,9,10	tCK (avg)	Reserved		ns
CL=6	CWL=5	tCK (avg)	2.5	3.3	ns
	CWL=6	tCK (avg)	Reserved		ns
	CWL=7,8,9,10	tCK (avg)	Reserved		ns
CL=7	CWL=5	tCK (avg)	Reserved		ns
	CWL=6	tCK (avg)	1.875	<2.5	ns
	CWL=7,8,9,10	tCK (avg)	Reserved		ns
CL=8	CWL=5	tCK (avg)	Reserved		ns
	CWL=6	tCK (avg)	1.875	<2.5	ns
	CWL=7,8,9,10	tCK (avg)	Reserved		ns
CL=9	CWL=5,6	tCK (avg)	Reserved		ns
	CWL=7	tCK (avg)	1.5	<1.875	ns
	CWL=8,9,10	tCK (avg)	Reserved		ns
CL=10	CWL=5,6	tCK (avg)	Reserved		ns
	CWL=7	tCK (avg)	1.5	<1.875	ns
	CWL=8,9,10	tCK (avg)	Reserved		ns
CL=11	CWL=5,6,7	tCK (avg)	Reserved		ns
	CWL=8	tCK (avg)	1.25	<1.5	ns
	CWL=9,10	tCK (avg)	Reserved		ns
CL=12	CWL=5,6,7,8,9	tCK (avg)	Reserved		ns
CL=13	CWL=5,6,7,8	tCK (avg)	Reserved		ns
	CWL=9	tCK (avg)	1.07	<1.25	ns
	CWL=10	tCK (avg)	Reserved		ns
CL=14	CWL=5,6,7,8	tCK (avg)	Reserved		ns
	CWL=9	tCK (avg)	0.938	<1.07	
Supported CL settings			5,6,7,8,9,10,11,13,14		nCK
Supported CWL settings			5,6,7,8,9,10		nCK

3.20. AC Timing Characteristics

Refer to section 13 in JEDEC Standard No. JESD79-3F.

[Table 15] AC Timing Characteristics 1

Parameter	Symbol	min/max	Data Rate				Unit
			1333	1600	1866	2133	MT/s
Max.Frequency			667	800	933	1066	MHz
Clock Timing							
Average clock period	tCK(avg)	min	1500	1250	1070	938	ps
		max	3333				ps
Minimum clock cycle time	tCK(DLL-off)	min	8				ps
Average High pulse width	tCH(avg)	min	0.47				tCK(avg)
		max	0.53				
Average Low pulse width	tCL(avg)	min	0.47				tCK(avg)
		max	0.53				
Absolute clock period	tCK(abs)	min	tCK(avg)min +tJIT(per)min				ns
		max	tCK(avg)max +tJIT(per)max				ns
Absolute High clock pulse width	tCH(abs)	min	0.43				tCK(avg)
Absolute Low clock pulse width	tCL(abs)	min	0.43				tCK(avg)
Command and Address Timing Parameters							
Active to read/write	tRCD	min	13.125				ns
Precharge command period	tRP	min	13.125				ns
Active to active/auto-refresh	tRC	min	49.125	48.125	47.125	47.125	ns
Active to precharge	tRAS	min	36	35	34	34	ns
		max	9×tREFI				ns
Control and Address input pulse width for leach input	tIPW	min	620	560	535	470	ps
Active bank A to Active bank B(×8)	tRRD(×8)	min	max(4nCK,6ns)				-
Active bank A to Active bank B(×16)	tRRD(×16)	min	max(4nCK,7.5ns)				-
Four active window(×8)	tFAW(×8)	min	30	30	27	25	ns
Four active window(×16)	tFAW(×16)	min	45	40	35	35	ns
Address and control input hold time (VIH/VIL(DC90)levels)	tIH(base) DC90	min	150	130	110	105	ps
Address and control input setip time (VIH/VIL(AC160)levels)	tIS(base) AC160	min	80	60	-	-	ps
Address and control input setip time (VIH/VIL(AC135)levels)	tIS(base) AC135	min	205	185	65	60	ps
Address and control input setip time (VIH/VIL(AC125)levels)	tIS(base) AC125	min	-	-	150	135	ps
/CAS to/CAS command delay	tCCD	min	4				nCK
Mode register set command cycle time	tMRD	min	4				nCK
Mode register set command update delay	tMOD	min	max(12nCK,15ns)				-
Write recovery time	tWR	min	15				ns
Auto precharge write recovery +precharge	tDAL	min	WR+RU(tRP/tCK(avg))				nCK
Multi-Purpose register Recovery time	tMPRR	min	1				nCK
Internal write to read command delay	tWTR	min	max(4nCK,7.5ns)				-
Internal read to precharge command delay	tRTP	min	max(4nCK,7.5ns)				-
Exit reset from CKE high to a valid command	tXPR	min	max(5nCK,tRFC(min)+10ns)				-
DLL locking time	tDLLK	min	512				nCK

[Table 16] AC Timing Characteristics 2

Parammr	Symbol	min/max	DataRat,				Unit
			1333	1600	1866	2133	MT/s
Max. Frequency			667	800	933	1066	MHz
DQ input Parameters							
DQ and OM input hold time (VIH/VIL (OC90) levels)	tDH(base) DC90 SR=1V/ns	min	75	55	-	-	ps
DQ and OM input hold time (VIH/VIL (OC90) levels)	tDH(base) DC90 SR=2V/ns	min	-	-	75	60	ps
DQ and OM input hold time (VIH/VIL (AC135) levels)	tDS(base) AC135 SR=1V/ns	min	45	25	-	-	ps
DQ and OM input hold time (VIH/VIL (AC130) levels)	tDS(base) AC130 SR=2V/ns	min	-	-	70	55	ps
DQ and OM input pulsen width for each input	tDIPW	min	400	360	320	280	ps
DQ output Parameters							
DQS, /DQS to OQ skew, per group, per access	tDQSQ	max	125	100	85	75	ps
DQ output hold time from DQS, /OQS	tQH	min	0.38				tCK(avg)
DQ high-impedance time	tHZ(DQ)	max	250	225	195	180	ps
DQ low-impedance time	tLZ(DQ)	min	-500	-450	-390	-360	ps
		max	250	225	195	180	ps
DQ strobe input Parameters							
DQS latching rising transitions to associated clock edge	tDQSS	min	-0.25	-0.27			tCK(avg)
		max	0.25	0.27			tCK(avg)
DQS input high pulse width	tDQSH	min	0.45				tCK(avg)
		max	0.55				tCK(avg)
DQS input low pulse width	tDQSL	min	0.45				tCK(avg)
		max	0.55				tCK(avg)
DQS falling edge hold time from rising CK	tDSH	min	0.2	0.18			tCK(avg)
DQS falling edge setup time from rising CK	tDSS	min	0.2	0.18			tCK(avg)
Write preamble	tWPRE	min	0.9				tCK(avg)
Write postamble	tWPST	min	0.3				tCK(avg)
DQ strobe output Parameters							
DQS, /DQS rising edge output access time from rising CK, /CK	tDQSCK	min	-255	-225	-195	-180	ps
		max	255	225	195	180	ps
DQS output high time	tQSH	min	0.4				tCK(avg)
DQS output low time	tQSL	min	0.4				tCK(avg)
DQS, /DQS high-impedance time IRL+B/2 referencel	tHZ(DQS)	max	250	225	195	180	ps
DQS, /DQS high-impedance time (RL + BL/2 reference)	tLZ(DQS)	min	-500	-450	-390	-360	ps
		max	250	225	195	180	ps
Read preamble	tRPRE	min	0.9				tCK(avg)
Read postamble	tRPST	min	0.3				tCK(avg)

[Table 17] AC Timing Characteristics 3

Parameter	Symbol	min/max	Data Rate				Unit
			1333	1600	1866	2133	MT/s
Max.Frequency			667	800	933	1066	MHz
Power-down Entry Parameters							
Timing of ACT command to power-down entry	tACTPDEN	min	1				nCK
Timing of Precharge/Precharge ALL command to power-down entry	tPRPDEN	min	1				nCK
Timing of Read/Read with auto-precharge command to nower-down entry	tPDPDEN	min	RL+4+1				nCK
Timing of Write command to power-down entry (BL80TF, BL8MRS, BC40TF)	tWRPDEN	min	WL+4+tWR/tCK(avg)				nCK
Timing of Write command to power-down entry (BC4MRS)		min	WL+2+tWR/tCK(avg)				nCK
Timing of Write with auto-precharge command to power-down entry (BL8OTF, BL8MRS, BC4OTE)	tWRAPDEN	min	WL+4+WR+1				nCK
Timing of Write with auto-precharge command to power-down entry (BC4MRS)		min	WL+2+WR+1				nCK
Timing of REF command to power-down entry	tREFPDEN	min	1				nCK
Timing of MRS command to power-down entry	tMRSPDEN	min	tMOD(min)				-
Exit precharge power-down with DLL frozen to command requiring a locked.DLL	tXPDLL	min	max(10nCK,24ns)				-
Exit power-down with DLL on to any valid command; Exit precharge power-down with DLL frozen to commands not requiring a lcoked DLL	tXP	min	max(3nCK,6ns)				-
CKE minimum pulse width (thigh and low oulse width)	tCKE	min	max(3nCK, 5.625ns)	max(3nCK,5ns)			-
Power-down entry to exit timing	tPD	min	tCKE(min)				-
		max	9xtREFI				-
Command pass disable delay	tCPDED	min	1		2	2	nCK
ODT to power-down entry/exit latency	tANPD	min	WL-1				-
Refresh Parameters							
Auto-refresh to Active/auto-refresh command	tRFC	min	160				ns
Average periodic refresh interval(TC ≤+85℃)	tREFI	max	7.8				μs
Average periodic refresh interval(TC>+85℃)			3.9				μs
Minimum CKE low width for self-refresh entry to exit timing	tCKESR	min	tCKE(min)+1nCK				-
Valid clock requirement after sele-refresh entry or power-down entry	tCKSRE	min	max(5nCK,10ns)				-
Valid clock requirement before self-refresh exit or power-down exit	tCKSRX	min	max(5nCK,10ns)				-
Exit self-refresh to commands not requiring a locked DLL	tXS	min	max(5nCK,tRFC(min)+10ns)				-
Exit self-refresh to commands requiring a lcock DLL	tXSDLL	min	tDLLK(min)				nCK

[Table 18] AC Timing Characteristics 4

Parameter	Symbol	min/max	Data Rate				Unit
			1333	1600	1866	2133	MT/s
Max.Frequency			667	800	933	1066	MHz
ODTTiming Parameters							
RTT turn-on	tAON	min	-250	-225	-195	-180	ps
		max	250	225	195	180	ps
Asynchronous RTT turn-on delay (Power-down with DU frozen)	tAONPD	min	2				ns
		max	8.5				ns
RTT_Nom and RTT_WR turn-off Time from ODTLoff reference	tAOF	min	0.3				tCK(avg)
		max	0.7				tCK(avg)
Asynchronous RTT turn-off delay (Power-down with DU frozen)	tAOFPD	min	2				ns
		max	8.5				ns
ODT turn-on latency	ODTon	-	WL-2				-
ODT turn-off latency	ODToff	-	WL-2				-
ODT latency for changing from RTT_Nom to RTT_WR	ODTLcnw	-	WL-2				-
ODT latency for changing from RTI_WR toRTT Nom(BC4)	ODTLcnw4	-	4+0DTLoff				nCK
ODT latency for changing from RTI_WR toRTT Nom(BL8)	ODTLcnw8	-	6+ ODTLoff				nCK
Minimum ODT high time after ODT asseretion or agter Write (BL4)	ODTH4	min	4				nCK
Minimum ODT high time after Write (BL8)	ODTH8	min	6				nCK
RTT change skew	tADC	min	0.3				tCK(avg)
		max	0.7				tCK(avg)
Calibration Timing Parameters							
Power-up and rest calibration time	tZQinit	min	max(512nCK, 640ns)				-
Normal operation full calibratio time	tZQoper	min	max(256nCK, 320ns)				-
Normal operation short calibratio time	tZQCS	min	max(64nCK, 80ns)				-
Write leveling Timing Parameters							
First OQS pulse rising edge after write leveling mode is programmed	tWLMRD	min	40				nCK
DOS, /DQS delay after write leveling mode is programmed	tWLDQSEN	min	25				nCK
Write leveling setup time from rising CK, /CK crossing to rising DQS /DOS crossing	tWLS	min	195	165	140	125	ps
Write leveling setup time from rising DOS, /DQS crossing to rising CK, /CK crossing	tWLH	min	195	165	140	125	ps
write leveling output delay	tWLO	min	0				ns
		max	9	7.5		7	ns
Write leveling output error	tWLOE	min	0				ns
		max	2				ns

[Table 19] AC Timing Characteristics 5

Parameter	Symbol	min/max	Data Rate				Unit
			1333	1600	1866	2133	MT/s
Max.Frequency			667	800	933	1066	MHz
Clock Jitter Specification							
Clock Period Jitter	tJIT(per)	min	-80	-70	-60	-50	ps
		max	80	70	60	50	
Maximum Clock Jitter between two consecutive	tJIT(cc)	max	160	140	120	100	ps
Duty cycle Jitter(with allowed jitter)	tJIT(duty)	min	-				ps
		max	-				
Cumulative error across 2 cycles	tERR(2per)	min	-118	-103	-88	-74	ps
		max	118	103	88	74	
Cumulative error across 3 cycles	tERR(3per)	min	-140	-122	-105	-87	ps
		max	140	122	105	87	
Cumulative error across 4 cycles	tERR(4per)	min	-155	-136	-117	-97	ps
		max	155	136	117	97	
Cumulative error across 5 cycles	tERR(5per)	min	-168	-147	-126	-105	ps
		max	168	147	126	105	
Cumulative error across 6 cycles	tERR(6per) allowed	min	-177	-155	-133	-111	ps
		max	177	155	133	111	
Cumulative error across 7 cycles	tERR(7per)	min	-186	-163	-139	-116	ps
		max	186	163	139	116	
Cumulative error across 8 cycles	tERR(8per)	min	-193	-169	-145	-121	ps
		max	193	169	145	121	
Cumulative error across 9 cycles	tERR(9per)	min	-200	-175	-150	-125	ps
		max	200	175	150	125	
Cumulative error across 10 cycles	tERR(10per)	min	-205	-180	-154	-128	ps
		max	205	180	154	128	
Cumulative error across 11 cycles	tERR(11per)	min	-210	-184	-158	-132	ps
		max	210	184	158	132	
Cumulative error across 12 cycles	tERR(12per)	min	-215	-188	-161	-134	ps
		max	215	188	161	134	
Cumulative error across n =13,14...49,50 cycles	tERR(nper)	min	tERR(nper)min.=(1+0.68ln(n))×tJIT(per)min.				ps
		max	tERR(nper)man.=(1+0.68ln(n))×tJIT(per)man.				

4. Functional Description and Timing

4.1. Simplified State Diagram

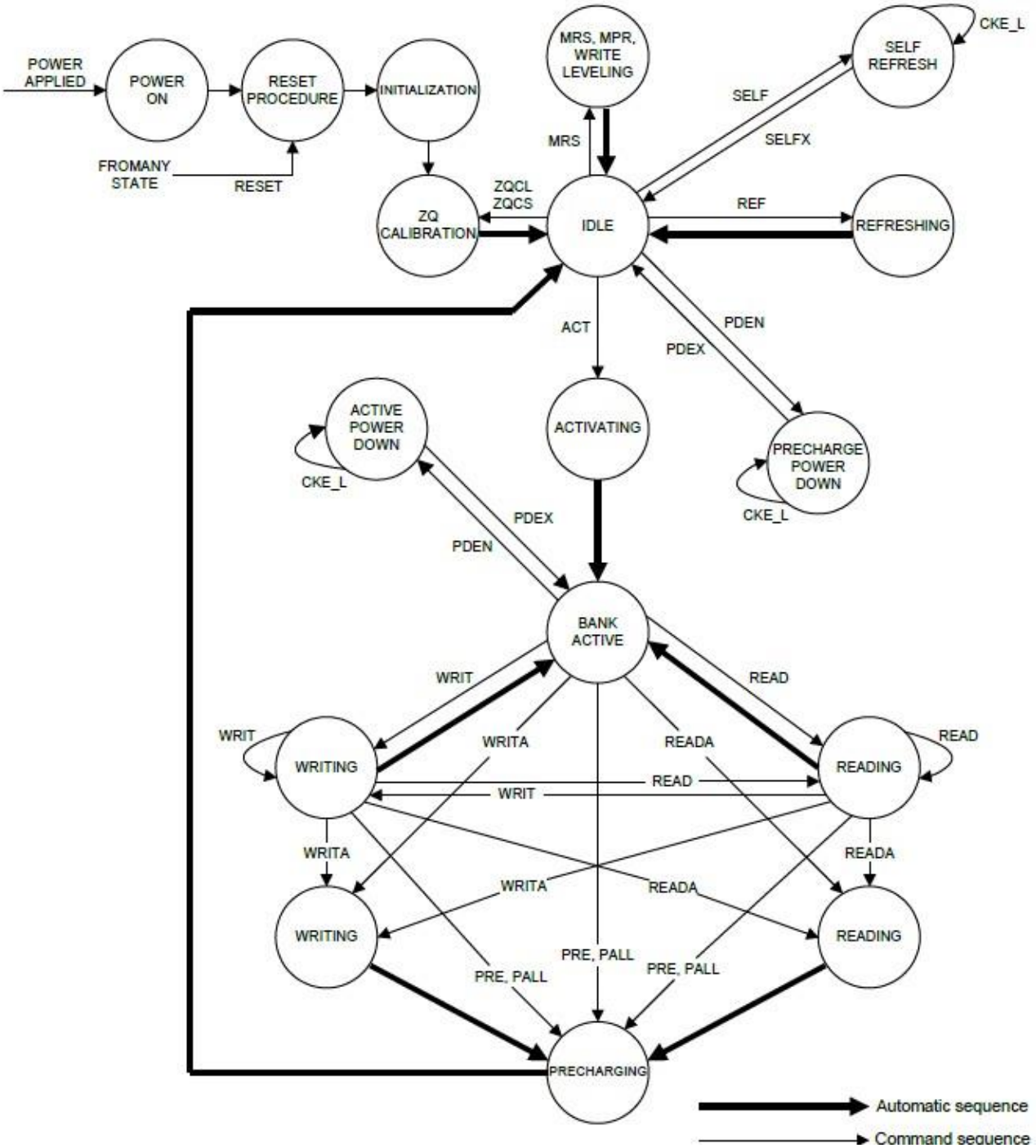


Figure 5 State Diagram

4.2. RESET and Initialization Procedure

Power-Up and Initialization Sequence

[1] Apply power

- /RESET is recommended to be maintained below 0.2 x VDD, all other inputs may be undefined. y /RESET needs to be maintained for minimum 200us with stable power. CKE is pulled low anytime before /RESET being de-asserted (min. time 10ns). The power voltage ramp time between 300mV to VDD (min.) must be no greater than 200ms; and during the ramp, VDD > VDDQ and (VDD - VDDQ) < 0.3V.
- VDD and VDDQ are driven from a single power converter output.

  AND
- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95V max once power ramp is finished.,

  AND
- VREF tracks VDDQ/2.

  OR
- Apply VDD without any slope reversal before or at the same time as VDDQ.
- Apply VDDQ without any slope reversal before or at the same time as VTT and VREF.
- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.

[2] After /RESET is de-asserted, wait for another 500us until CKE become active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.

[3] Clocks (CK, /CK) need to be started and stabilized for at least 10ns or 5tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (tIS) must be met. Also a NOP or DESL command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE registered "high" after Reset, CKE needs to be continuously registered high until the initialization sequence is finished, including expiration of tDLLK and tZQinit.

[4] The DDR3 SDRAM will keep its on-die termination in high-impedance state during /RESET being asserted at least until CKE being registered high. Therefore, the ODT signal may be in undefined state until tIS before CKE being registered high. After that, the ODT signal must be kept inactive (low) until the power-up and initialization sequence is finished, including expiration of tDLLK and tZQinit.

[5] After CKE being registered high, wait minimum of tXPR, before issuing the first MRS command to load mode register. (tXPR = max. (tXS ; 5 x tCK))

[6] Issue MRS command to load MR2 with all application settings. (To issue MRS command for MR2, provide low to BA0 and BA2, high to BA1.)

[7] Issue MRS command to load MR3 with all application settings. (To issue MRS command for MR3, provide low to BA2, high to BA0 and BA1.)

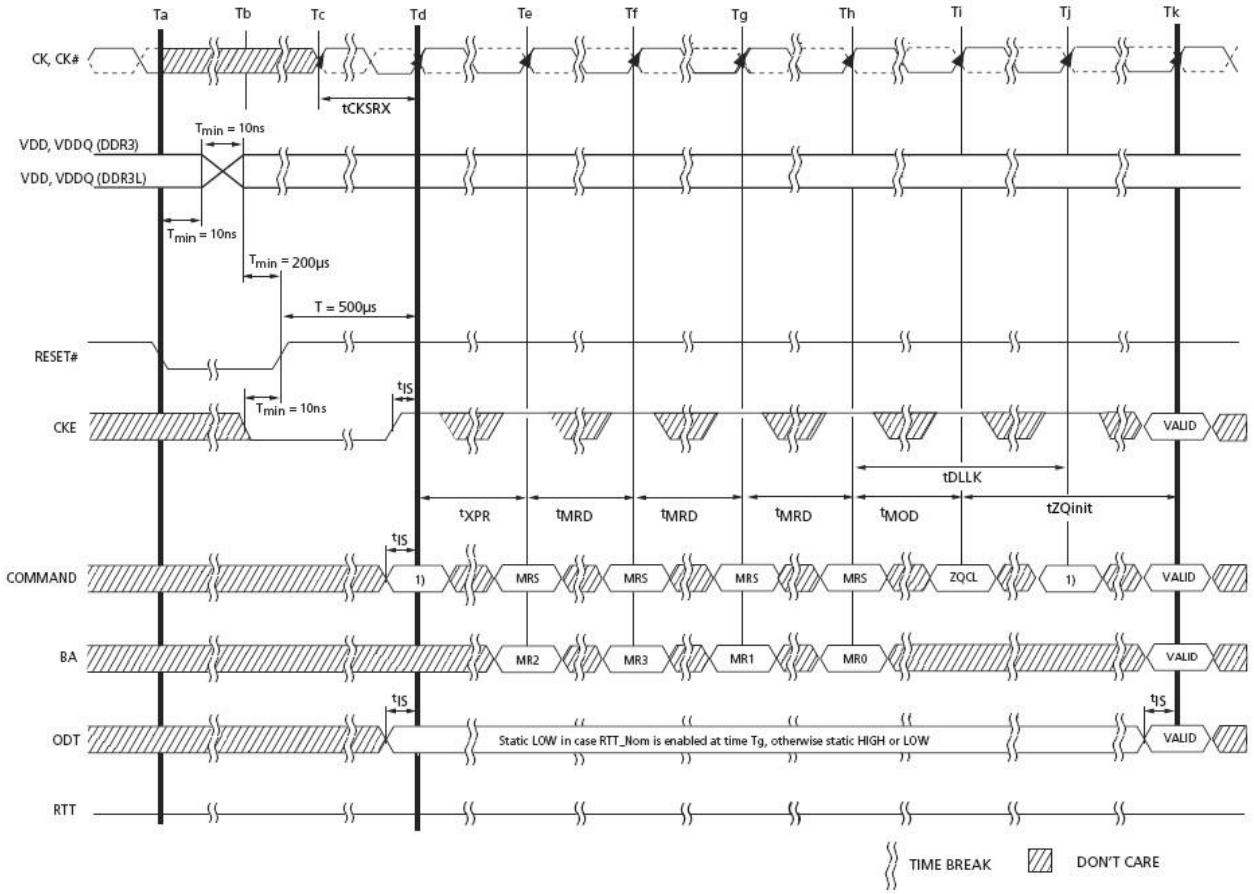
[8] Issue MRS command to load MR1 with all application settings and DLL enabled. (To issue DLL Enable command, provide low to A0, high to BA0 and low to BA1 and BA2.)

[9] Issue MRS command to load MR0 with all application settings and DLL reset. (To issue DLL reset command, provide high to A8 and low to BA0 to BA2.)

[10] Issue ZQCL command to start ZQ calibration.

[11] Wait for both tDLLK and tZQinit completed.

[12] The DDR3 SDRAM is now ready for normal operation.



Note: From time point Td until Tk, NOP or DES commands must be applied between MRS and ZQCL commands.

Figure 6 Reset Procedure at Power Stable Condition

4.3. Programming the Mode Register

For application flexibility, various functions, features and modes are programmable in four mode registers, provided by the DDR3 SDRAM, as user defined variables, and they must be programmed via a Mode Register Set (MRS) command. As the default values of the Mode Registers (MR#) are not defined, content of mode registers must be fully initialized and/or reinitialized, i.e. written, after Power-up and/or reset for proper operation. Also the contents of the mode registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset does not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents.
The mode register set command cycle time, tMRD is required to complete the write operation to the mode register and is the minimum time required between two MRS commands. The MRS command to non-MRS command delay, tMOD, is required for the DRAM to update the features except DLL reset and is the minimum time required from an MRS command to a non-MRS command excluding NOP and DESL. The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e. all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is already high prior to writing into the mode register. The mode registers are divided into various fields depending on the functionality and/or modes.

Mode Register Set Command Cycle Time (tMRD)

tMRD is the minimum time required from an MRS command to the next MRS command. As DLL enable and DLL reset are both MRS commands, tMRD is applicable between MRS to MR1 for DLL enable and MRS to MR0 for DLL reset, and not tMOD.

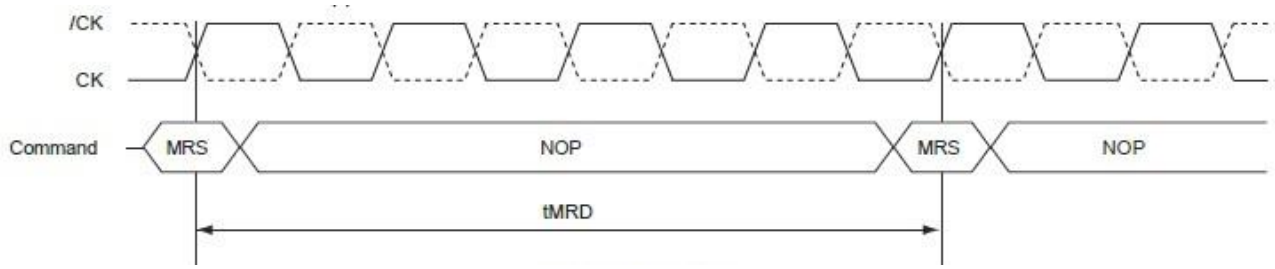


Figure 7 tMRD Timing

MRS Command to Non-MRS Command Delay (tMOD)

tMOD is the minimum time required from an MRS command to a non-MRS command excluding NOP and DESL. Note that additional restrictions may apply, for example, MRS to MR0 for DLL reset followed by read.

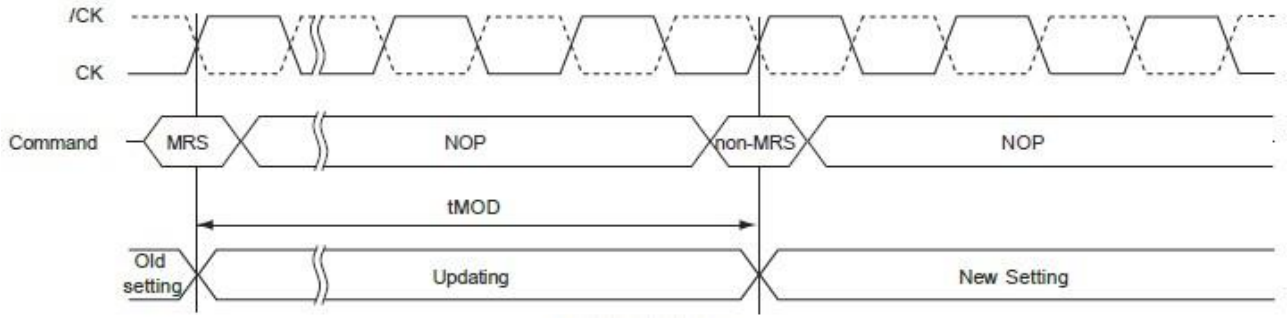
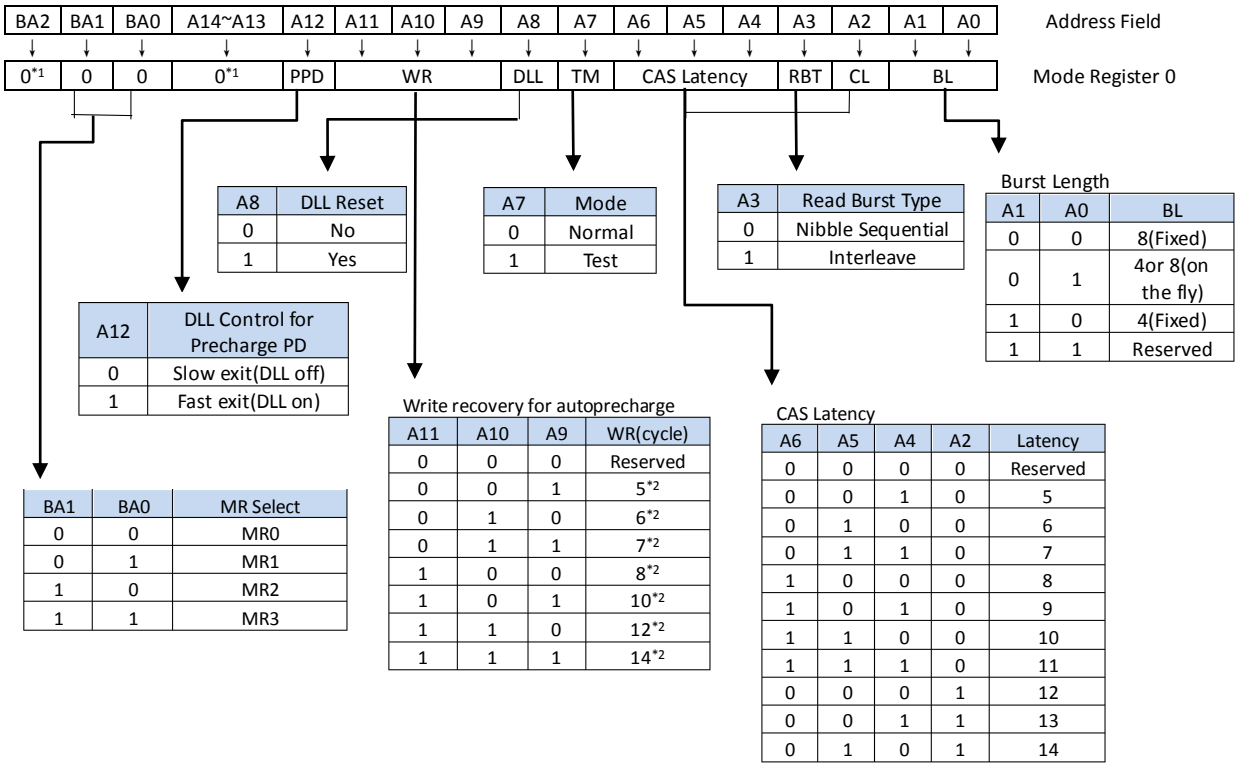


Figure 8 tMOD Timing

4.4. DDR3 SDRAM Mode Register 0 [MR0]

The Mode Register MR0 stores the data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, /CAS latency, test mode, DLL reset, WR and DLL control for precharge power-down, which include various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on /CS, /RAS, /CAS, /WE, BA0, BA1 and BA2, while controlling the states of address pins according to the table below.



A8	DLL Reset
0	No
1	Yes

A7	Mode
0	Normal
1	Test

A3	Read Burst Type
0	Nibble Sequential
1	Interleave

A1	A0	BL
0	0	8(Fixed)
0	1	4or 8(on the fly)
1	0	4(Fixed)
1	1	Reserved

A12	DLL Control for Precharge PD
0	Slow exit(DLL off)
1	Fast exit(DLL on)

BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A11	A10	A9	WR(cycle)
0	0	0	Reserved
0	0	1	5*2
0	1	0	6*2
0	1	1	7*2
1	0	0	8*2
1	0	1	10*2
1	1	0	12*2
1	1	1	14*2

A6	A5	A4	A2	Latency
0	0	0	0	Reserved
0	0	1	0	5
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11
0	0	0	1	12
0	0	1	1	13
0	1	0	1	14

Figure 9 MR0 Programming

Notes:
[1] BA2 and A13 ~ A14 are reserved for future use and must be programmed to 0 during MRS.
[2] WR (Write Recovery for auto-precharge) min in clock cycle is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer:
[3] WR min [cycles] = roundup (tWR [ns] / tCK [ns]).
[4] The WR value in the mode register must be programmed to be equal or larger than WR min. The programmed WR value is used with tRP to determine tDAL.

4.5. DDR3 SDRAM Mode Register 1 [MR1]

The Mode Register MR1 stores the data for enabling or disabling the DLL, output driver strength, RTT_Nom impedance, additive latency, write leveling enable and Qoff. The Mode Register 1 is written by asserting low on /CS, /RAS, /CAS, /WE, high on BA0 and low on BA1, while controlling the states of address pins according to the table below.

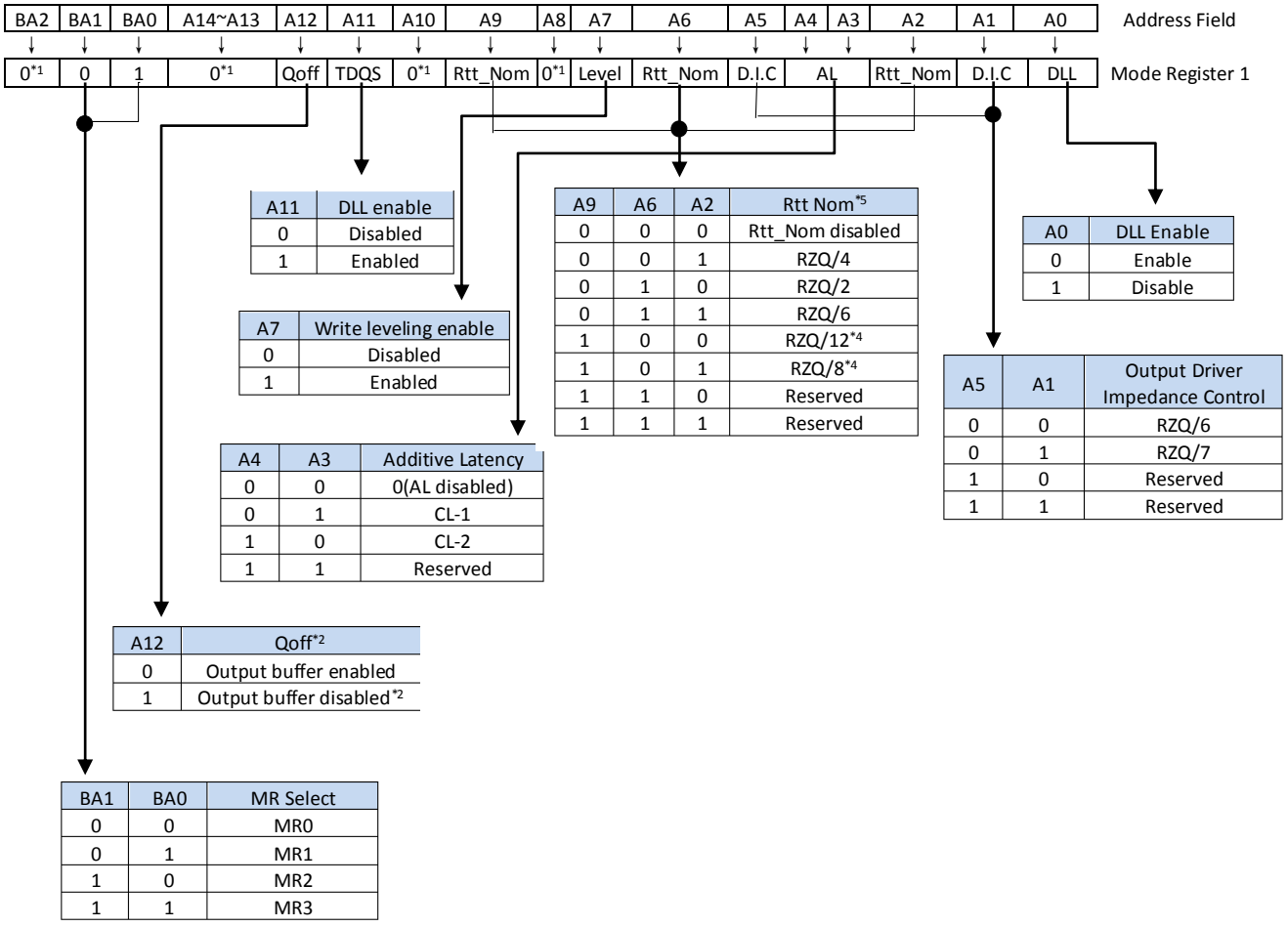
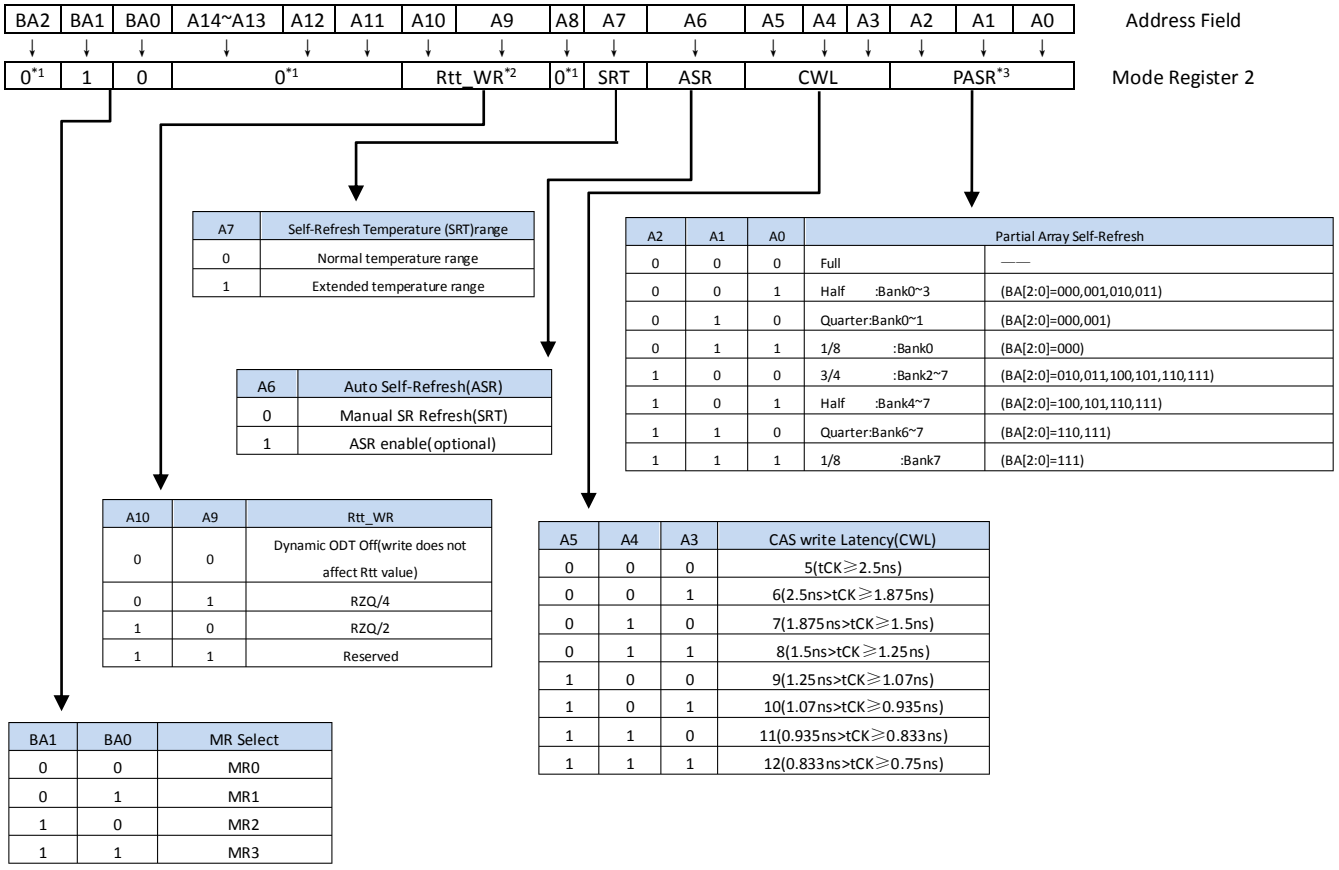


Figure 10 MR1 Programming

Notes:
[1] BA2, A8, A10, A11 and A13 ~ A14 are reserved for future use (RFU) and must be programmed to 0 during MRS.
[2] Outputs disabled - DQ, DQS, /DQS.
[3] RZQ = 240 Ohm.
[4] If RTT_Nom is used during writes, only the values RZQ/2, RZQ/4 and RZQ/6 are allowed. [5] In write leveling mode (MR1[bit7] = 1) with MR1[bit12] = 1, all RTT_Nom settings are allowed; in write leveling mode (MR1[bit7] = 1) with MR1[bit12] = 0, only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.

4.6. DDR3 SDRAM Mode Register 2 [MR2]

The Mode Register MR2 stores the data for controlling refresh related features, RTT_WR impedance and /CAS write latency (CWL). The Mode Register 2 is written by asserting low on /CS, /RAS, /CAS, /WE, high on BA1 and low on BA0, while controlling the states of address pins according to the table below.



A7	Self-Refresh Temperature (SRT)range
0	Normal temperature range
1	Extended temperature range

A6	Auto Self-Refresh(ASR)
0	Manual SR Refresh(SRT)
1	ASR enable(optional)

A10	A9	Rtt_WR
0	0	Dynamic ODT Off(write does not affect Rtt value)
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A2	A1	A0	Partial Array Self-Refresh	
0	0	0	Full	——
0	0	1	Half :Bank0~3	(BA[2:0]=000,001,010,011)
0	1	0	Quarter:Bank0~1	(BA[2:0]=000,001)
0	1	1	1/8 :Bank0	(BA[2:0]=000)
1	0	0	3/4 :Bank2~7	(BA[2:0]=010,011,100,101,110,111)
1	0	1	Half :Bank4~7	(BA[2:0]=100,101,110,111)
1	1	0	Quarter:Bank6~7	(BA[2:0]=110,111)
1	1	1	1/8 :Bank7	(BA[2:0]=111)

A5	A4	A3	CAS write Latency(CWL)
0	0	0	5(tCK≥2.5ns)
0	0	1	6(2.5ns>tCK≥1.875ns)
0	1	0	7(1.875ns>tCK≥1.5ns)
0	1	1	8(1.5ns>tCK≥1.25ns)
1	0	0	9(1.25ns>tCK≥1.07ns)
1	0	1	10(1.07ns>tCK≥0.935ns)
1	1	0	11(0.935ns>tCK≥0.833ns)
1	1	1	12(0.833ns>tCK≥0.75ns)

Figure 11 MR2 Programming

Notes:
[1] BA2, A8 and A11 to A14 are RFU and must be programmed to 0 during MRS.
[2] The Rtt_WR value can be applied during writes even when Rtt_Nom is desabled. During write leveling, Dynamic ODT is not available.
[3] Optional in DDR3 SDRAM: If PASR (Partial Array Self-Refresh) is enabled, data located in areas of the array beyond the specified address range will be lost if self-refresh is entered. Data integrity will be maintained if tREF conditions are met and no self-refresh command is issued.

4.7. DDR3 SDRAM Mode Register 3 [MR3]

The Mode Register MR3 controls Multi Purpose Registers (MPR). The Mode Register 3 is written by asserting low on /CS, /RAS, /CAS, /WE, high on BA1 and BA0, while controlling the states of address pins according to the table below.

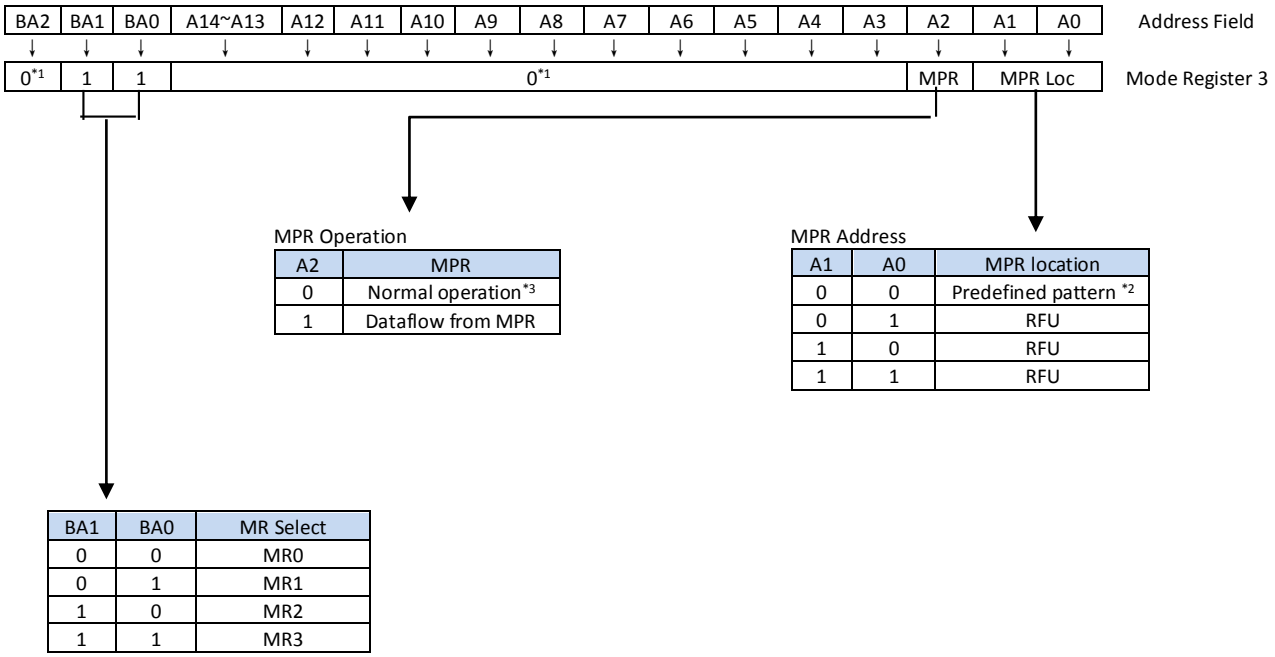


Figure 12 MR3 Programming

Notes:
[1] BA2, A3 to A14 are reserved for future use (RFU) and must be programmed to 0 during MRS.
[2] The predefined pattern will be used for read synchronization.
[3] When MPR control is set for normal operation, MR3 A[2]=0, MR3 A[1:0] will be ignored.

4.8. Extended Temperature Usage

[Table 20] Mode Register Description

Field	Bits	Description
ASR	MR2(A6)	Auto Self-Refresh (ASR) when enabled, DDR3 SDRAM automatically provides Self-Refresh power management functions for all supported operating temperature values. If not enabled, the SRT bit must be programmed to indicate TC during subseauent Self-Refresh operation 0=Manual SR Reference(SRT) 1=ASR enable
SRT	MR2(A7)	Self-Refresh Temperature (SRT) Range If ASR =0, the SRT bit must be programmed to indicate TC during subsequent Self-Refresh operation If ASR=1. SRT bit must be set to Ob 0=Normal operating temperature range 1=Extended(optional) operating temperature range

Partial Array Self-Refresh (PASR)

Optional in DDR3 SDRAM: Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material. If PASR (Partial Array Self-Refresh) is enabled, data located in areas of the array beyond the specified address range shown in figure of MR2 programming will be lost if Self-Refresh is entered. Data integrity will be maintained if tREFI conditions are met and no Self-Refresh command is issued.

Auto Self-Refresh Mode - ASR Mode

DDR3 SDRAM provides an Auto Self-Refresh mode (ASR) for application ease. ASR mode is enabled by setting MR2 bit A6 = 1 and MR2 bit A7 = 0. The DRAM will manage self-refresh entry in either the Normal or Extended (optional) Temperature Ranges. In this mode, the DRAM will also manage self-refresh power consumption when the DRAM operating temperature changes, lower at low temperatures and higher at high temperatures.

If the ASR option is not supported by the DRAM, MR2 bit A6 must be set to 0.
If the ASR mode is not enabled (MR2 bit A6 = 0), the SRT bit (MR2 A7) must be manually programmed with the operating temperature range required during self-refresh operation. Support of the ASR option does not automatically imply support of the Extended Temperature Range.

Self- Refresh Temperature Range - SRT

If ASR = 0, the Self-Refresh Temperature (SRT) Range bit must be programmed to guarantee proper self-refresh operation.
If SRT = 0, then the DRAM will set an appropriate refresh rate for self-refresh operation in the Normal Temperature Range.
If SRT = 1 then the DRAM will set an appropriate, potentially different, refresh rate to allow self-refresh operation in either the Normal or Extended Temperature Ranges. The value of the SRT bit can effect self-refresh power consumption, please refer to the IDD table for details.
For parts that do not support the Extended Temperature Range, MR2 bit A7 must be set to 0 and the DRAM should not be operated outside the Normal Temperature Range.

[Table 21] Self-Refresh Mode Summary

MR2 A[6]	MR2 A[7]	Self-Refresh operation	Allowed Operating Temperature Range for Self-Refresh Mode
0	0	Self-refresh rate appropriate for the Normal Temperature Range	Normal (0-85℃)
0	1	Self-refresh rate appropriate for either the Normal or Extended Temperature Ranges. The DRAM must support Extended Temperature Range. The value of the SRT bit can effect self-refresh power consumption, please refer to the IDD table for details.	Normal and Extended (0-95℃)
1	0	ASR enabled.Self-Refresh power consumption is temperature dependent	Normal(0-85℃)
1	0	ASR enabled.Self-Refresh power consumption is temperature dependent	Normal and Extended(0-95℃)
1	1	Illegal	

4.9. Refresh Command

The refresh command (REF) is used during normal operation of the DDR3 SDRAMs. This command is non- persistent, so it must be issued each time a refresh is required. The DDR3 SDRAM requires refresh cycles at an average periodic interval of tREFI. When /CS, /RAS and /CAS are held low and /WE high at the rising edge of the clock, the chip enters a refresh cycle. All banks of the SDRAM must be precharged and idle for a minimum of the precharge time tRP(min) before the refresh command can be applied. The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during a refresh command. An internal address counter supplies the addresses during the refresh cycle. No control of the external address bus is required once this cycle has started. When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the refresh command and the next valid command, except NOP or DESL, must be greater than or equal to the minimum refresh cycle time tRFC(min) as shown in the following figure. Note that the tRFC timing parameter depends on memory density.
In general, a refresh command needs to be issued to the DDR3 SDRAM regularly every tREFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of 8 refresh commands can be postponed during operation of the DDR3 SDRAM, meaning that at no point in time more than a total of 8 refresh commands are allowed to be postponed. In case that 8 refresh commands are postponed in a row, the resulting maximum interval between the surrounding refresh commands is limited to 9 × tREFI. A maximum of 8 additional refresh commands can be issued in advance ("pulled in"), with each one reducing the number of regular refresh commands required later by one. Note that pulling in more than 8 refresh commands in advance does not further reduce the number of regular refresh commands required later, so that the resulting maximum interval between two surrounding refresh commands is limited to 9 × tREFI. At any given time, a maximum of 16 REF commands can be issued within 2 × tREFI.
Self-refresh mode may be entered with a maximum of eight refresh commands being postponed. After exiting self-refresh mode with one or more refresh commands postponed, additional refresh commands may be postponed to the extent that the total number of postponed refresh commands (before and after the self-refresh) will never exceed eight. During self-refresh mode, the number of postponed or pulled-in REF commands does not change.

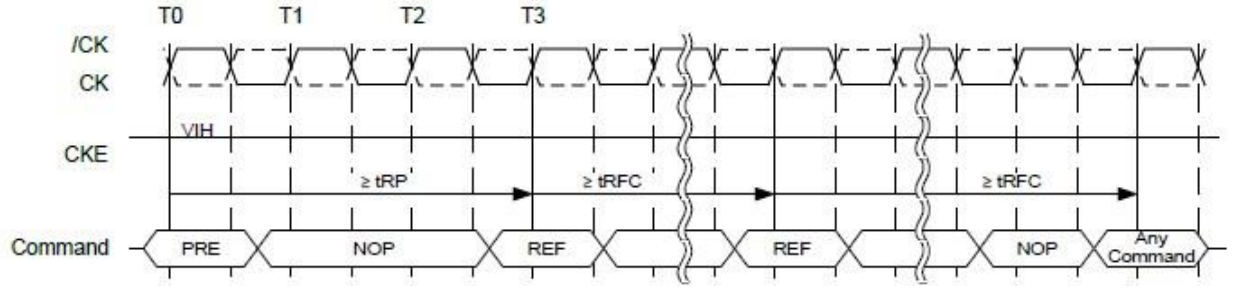


Figure 13 Refresh Command Timing

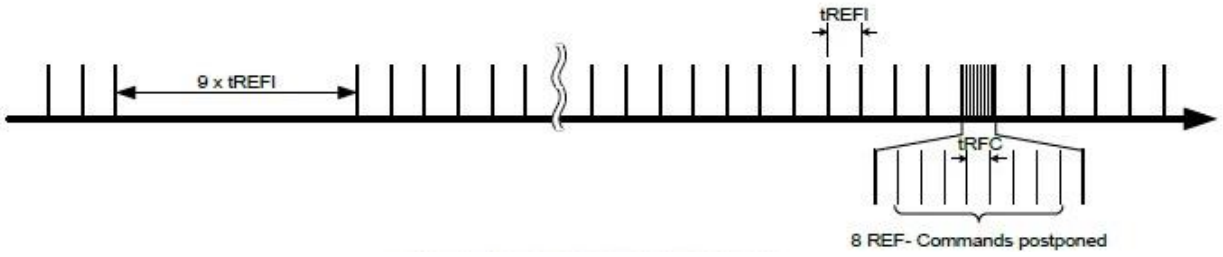


Figure 14 Postponing Refresh Commands

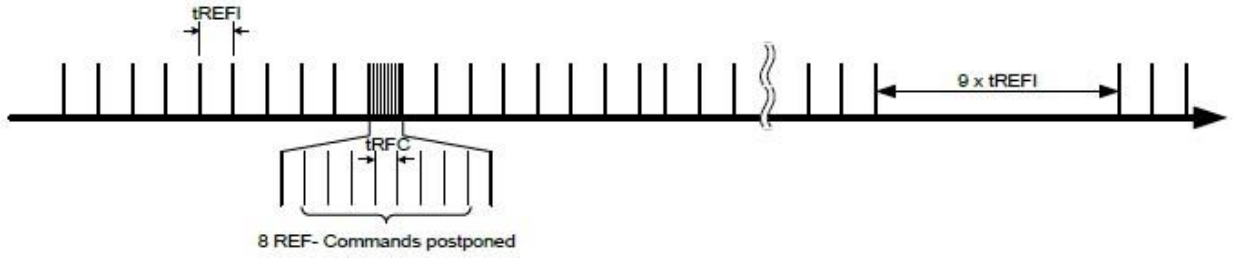


Figure 15 Pulling-in Refresh Commands

4.10. Self-Refresh Operation

The self-refresh command can be used to retain data in the DDR3 SDRAM, even if the rest of the system is powered down. When in the self-refresh mode, the DDR3 SDRAM retains data without external clocking. The DDR3 SDRAM device has a built-in timer to accommodate self-refresh operation. The self-refresh entry (SELF) command is defined by having /CS, /RAS, /CAS and CKE held low with /WE high at the rising edge of the clock.

Before issuing the self-refresh entry command, the DDR3 SDRAM must be idle with all bank precharge state with tRP satisfied. 'Idle state' is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) Also, on-die termination must be turned off before issuing self-refresh entry command, by either registering ODT pin low "ODTL + 0.5tCK" prior to the self-refresh entry command or using MRS to MR1 command. Once the self-refresh entry command is registered, CKE must be held low to keep the device in self-refresh mode. During normal operation (DLL on), MR1 (A0 = 0), the DLL is automatically disabled upon entering self-refresh and is automatically enabled (including a DLL-Reset) upon exiting self-refresh.

When the DDR3 SDRAM has entered self-refresh mode all of the external control signals, except CKE and /RESET, are "don't care". For proper self-refresh operation, all power supply and reference pins (VDD, VDDQ, VSS, VSSQ, VREFCA and VREFDQ) must be at valid levels. VREFDQ supply may be turned OFF and VREFDQ may take any value between VSS and VDD during self-refresh operation, provided that VREFDQ is valid and stable prior to CKE going back high and that first write operation or first write leveling activity may not occur earlier than 512 nCK after exit from self-refresh.

The DRAM initiates a minimum of one refresh command internally within tCKESR period once it enters self-refresh mode.

The clock is internally disabled during self-refresh operation to save power. The minimum time that the DDR3 SDRAM must remain in self-refresh mode is tCKESR. The user may change the external clock frequency or halt the external clock tCKSRE cycles after self-refresh entry is registered, however, the clock must be restarted and stable tCKSRX clock cycles before the device can exit self-refresh operation.

To protect DRAM internal delay on CKE line to block the input signals, one NOP (or DESL) command is needed after self-refresh entry.
The procedure for exiting self-refresh requires a sequence of events. First, the clock must be stable prior to CKE going back high. Once a self-refresh exit command (SREX, combination of CKE going high and either NOP or DESL on command bus) is registered, a delay of at least tXS must be satisfied before a valid command not requiring a locked DLL can be issued to the device to allow for any internal refresh in progress.
Before a command that requires a locked DLL can be applied, a delay of at least tXSDLL must be satisfied.
Depending on the system environment and the amount of time spent in self-refresh, ZQ calibration commands may be required to compensate for the voltage and temperature drift as described in ZQ Calibration section. To issue ZQ calibration commands, applicable timing requirements must be satisfied (See Figure ZQ Calibration).
CKE must remain high for the entire self-refresh exit period tXSDLL for proper operation except for self-refresh re-entry. Upon exit from self-refresh, the DDR3 SDRAM can be put back into self-refresh mode after waiting at least tXS period and issuing one refresh command (refresh period of tRFC). NOP or DESL commands must be registered on each positive clock edge during the self-refresh exit interval tXS. ODT must be turned off during tXSDLL.
The use of self-refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from self-refresh mode. Upon exit from self-refresh, the DDR3 SDRAM requires a minimum of one extra refresh command before it is put back into self-refresh mode.

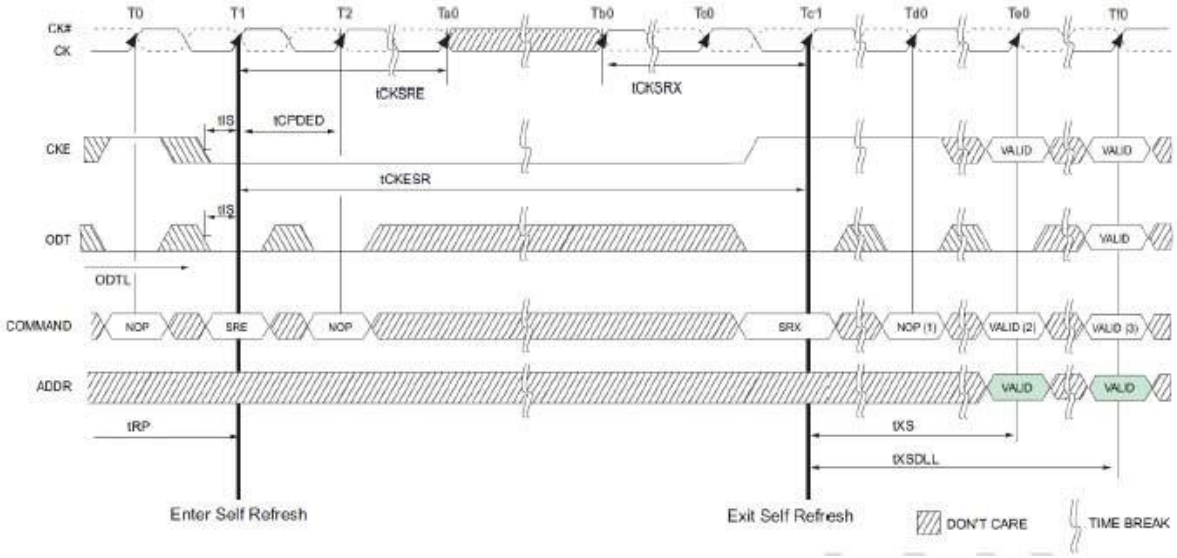


Figure 16 Self-Refresh Entry and Exit Timing

Notes:
[1] Only NOP or DESL commands.
[2] Valid commands not requiring a locked DLL.
[3] Valid commands requiring a locked DLL.
[4] One NOP or DESL commands.

4.11. DLL-off Mode

[Refer to section 4.5 in JEDEC Standard No. JESD79-3F]

4.12. DLL on/off switching procedure

[Refer to section 4.6 in JEDEC Standard No. JESD79-3F]

4.13. Input clock frequency change

[Refer to section 4.7 in JEDEC Standard No. JESD79-3F]

4.14. Write Leveling

[Refer to section 4.8 in JEDEC Standard No. JESD79-3F]

4.15. Multi Purpose Register

[Refer to section 4.10 in JEDEC Standard No. JESD79-3F]

4.16. Read Operation

[Refer to section 4.13 in JEDEC Standard No. JESD79-3F]

4.17. Write Operation

[Refer to section 4.14 in JEDEC Standard No. JESD79-3F]

4.18. Power-Down Modes

[Refer to section 4.17 in JEDEC Standard No. JESD79-3F]

4.19. On-Die Termination (ODT)

[Refer to section 5 in JEDEC Standard No. JESD79-3F]

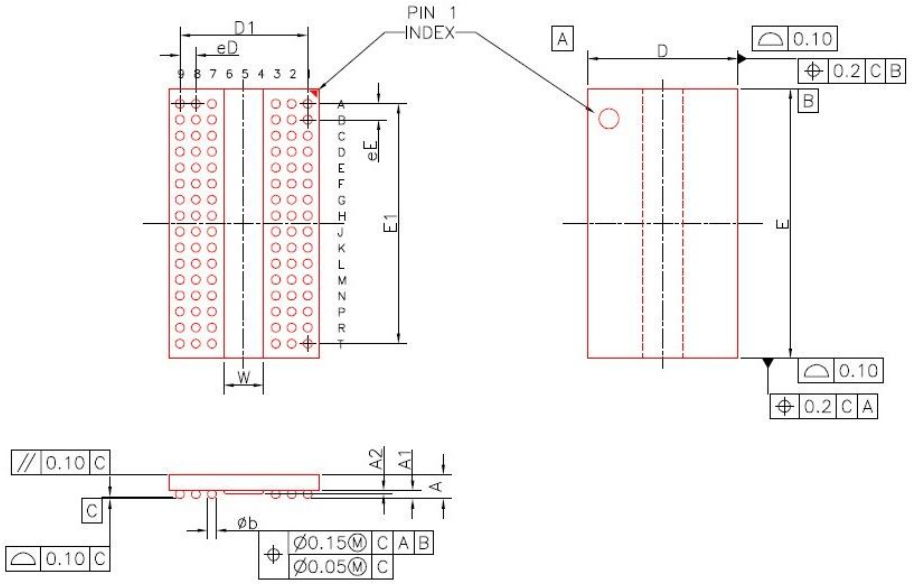
4.20. ZQ Calibration

[Refer to section 5.5 in JEDEC Standard No. JESD79-3F]

5. Physical Diagram

5.1. FBGA 96-ball 7.5mm×13.5mm

Unit :mm



Symbol	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.30	0.35	0.40
A2	0.10	0.15	0.20
D	7.40	7.50	7.60
D1	6.40 BSC		
E	13.40	13.50	13.60
E1	12.00 BSC		
b	0.40	0.45	0.50
eD	0.80 BSC		
eE	0.80 BSC		
W	1.95	2.00	2.05

Figure 17 FBGA 96-ball package outline drawing